Digital Flight Control Research Using Microprocessor Technology

ROBERT F. STENGEL
Princeton University

Abstract

The Flight Research Laboratory at Princeton University is engaged in an experimental program to investigate a variety of approaches to digital control by actual flight test. Experimentation is being conducted with Princeton's 6-DOF variable-response research aircraft (VRA), which is equipped for direct side-force control, direct-lift control, feedback of all motion variables, and multiple-pilot command modes. VRA avionics have been augmented by a microprocessor digital flight control system (Micro-DFCS), which uses off-the-shelf computer components capable of operating in parallel or in series with the existing variable-response system. The digital control laws operate in conjunction either with the "bare airframe" dynamics of the VRA or with the dynamics of a simulated aircraft, provided by the existing variable-response system. The initial flight control computer program CAS-1 provides three longitudinal control options: direct (unaugmented) command, pitch rate command, and normal acceleration command. The latter two options are "Type 0" systems designed by linear-quadratic control theory. Future Micro-DFCS software will provide a variety of increasingly complex control options, including "Type 1" logic, gain scheduling, coupled 3-axis control, and "CCV" command modes.

Manuscript received November 10, 1978.

This work was supported by the Office of Naval Research under Contract N00014-78-C-0257.

This paper was presented at the Flight Control Systems Criteria Symposium, Naval Postgraduate School, Monterey, Calif., July 1978.

Author's address: Department of Mechanical and Aerospace Engineerins, Princeton University, Princeton, N.J. 08540.

0018-9251/79/0500-0397 $00.75

Introduction

Research which anticipates the capabilities of emerging flight control technologies and establishes corresponding flight control system criteria plays a vital role in maintaining aeronautical progress. The needed research can begin on paper, but experiment and demonstration in flight are necessary for a full understanding of the relationships between control theory and practice.

Modern control theory and digital microprocessors represent two emerging technologies in the flight control context, and both must be tested in flight as a logical step to acceptance. Although "modern" control theory, which combines state space, time domain, and optimal control concepts with earlier frequency domain methods, has been with us for about two decades, there have been few applications of this theory to the *flight-critical* control of actual aircraft. (References [1] to [4] document programs that have used modern control laws in flight, and there may be other examples not cited here.) The commercial availability of single-board microcomputers is sufficiently recent that the application of microprocessors to flight control still is in its infancy. Past digital flight control programs, e.g., [2]-[9] have used pre-large-scale integration (pre-LSI) electronic technology, and while microprocessors are beginning to appear in navigation systems for general aviation, there have been no published examples of their applications to controlling manned aircraft. (Reference [10] indicates that the NASA HiMAT remotely piloted research vehicle, which is scheduled to fly this year, will use a microprocessor in its backup flight control system.)

The Flight Research Laboratory (FRL) at Princeton University is conducting an experimental program whose objectives combine research on advanced flight control concepts and their implementation with a microprocessor-based digital flight control system (Micro-DFCS). Although the project has been underway for less than half a year, the Micro-DFCS is installed in the research aircraft, the initial linear-optimal flight control law has been coded, and flight testing has begun. This paper describes the research systems, the present and future flight control software, and the research status of the program. With Office of Naval Research (ONR) sponsorship, FRL has identified and initiated a low-cost research project which will assist the Navy in evaluating flight control systems criteria and in designing digital flight control systems for future aircraft.

Research Systems

The primary experimental elements of this research program are the variable-response research aircraft (VRA), the Micro-DFCS, and the ground support systems. The VRA is a highly modified Navion equipped with inertial, air data, and navigation sensors, as well as six independent force and moment controls. The heart of the Micro-DFCS is a flight control computer unit

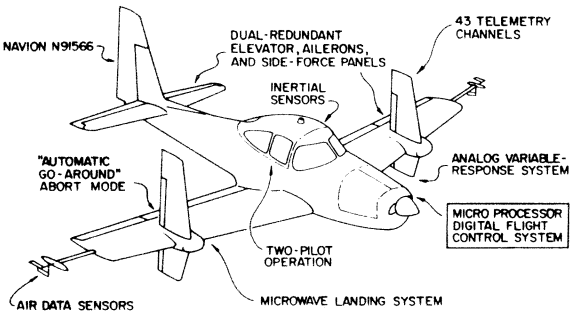


Fig. 1. Variable-response research aircraft (VRA).

TABLE I
VRA Control Characteristics

Control	Displacement Limit (deg)	Rate Limit (deg/s)	Bandwidth H_z	Maximum Specific Force or Moment (IAS = 70 knots)
Roll	30	70	5 (10)	4.1 rad/s^2
Pitch	−30 +15	70	5 (10)	4.4 rad/s^2
Yaw	15	70	5 (10)	1.9 rad/s^2
Thrust	-	-	0.6	0.1g
Side force	35	60	2 (3)	0.25g
Normal force	30	110	2 (3)	0.5g

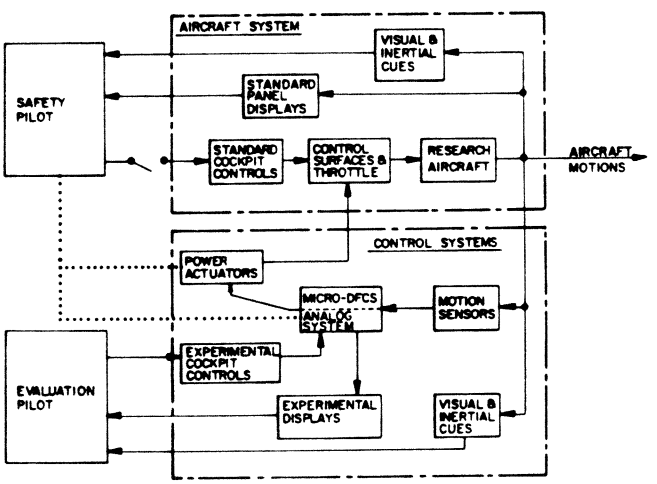


Fig. 2. Overview of VRA/Micro-DFCS System.

assembled at the Flight Research Laboratory from commercially available components. The ground support systems include equipment for flight simulation and software development, plus the FRL flight test facility. Each of these is discussed in more detail below.

Variable-Response Research Aircraft (VRA)

The VRA, shown in Fig. 1, has been used to conduct a broad range of experiments in aircraft flying qualities, human factors, and control in the past. The aircraft has played a major role in establishing current military and civil flying qualities criteria, and with the addition of the Micro-DFCS, the VRA is equipped to expand this type of research, as well as to investigate advanced digital control concepts.

Independent control of three forces and three moments is provided by commands to the elevator, ailerons, rudder, throttle, direct-lift flaps, and side-force panels. The control surfaces are driven by hydraulic servos originally fitted to the B-58 aircraft. The modified VRA units incorporate solenoid-actuated valves with force-override features for quick disengagement. Characteristics of the control effectors are summarized in Table I. Surface rate limits are seen to range from 60 to 110 deg/s. Bandwidths are given for flat response and 6-dB attenuation (in parentheses), except that thrust bandwidth is specified by the frequency for 3dB attenuation. The aircraft's normal operating speed range is 65 to 120 knots; maximum specific forces and moments ("control power") are given for 70-knots airspeed. At an indicated airspeed (IAS) of 105 knots, maximum direct lift and side-force accelerations are 1 g and 0.5 g, respectively.

The sensors used for most flight testing include angular rate gyros and linear accelerometers for all three axes, vertical and heading gyros, dual angle-of-attack and sideslip-angle vanes, radar altimeter, indicated airspeed, control surface positions, and cockpit control positions. Several other signals, e.g., air temperature, barometric altimeter, altitude rate, and TALAR microwave landing system signals, are available for system feedback or telemetry recording. The present telemetry system allows 42 data channels (plus voice) to be multiplexed and transmitted to the FRL ground station described below.

The general arrangement of VRA systems is shown in Fig. 2. The aircraft is flown by a two-man crew during all research. This provides a number of advantages in comparison to single-pilot operation from the standpoint of flight safety and experimental efficiency. The conventional mechanical aircraft system is flown by the safety pilot, while the fly-by-wire aircraft system used for research is flown by the evaluation pilot. This system includes the Micro-DFCS and redundant aileron, elevator, and side-force actuators for protection against system failures. The evaluation pilot's station is tailored to the experiment; for the Micro-DFCS program, this system includes a center control stick, thumb switches for trim and direct force modes, rudder pedals, sideslip and side-force-panel meters, and conventional instruments.

The safety pilot is the in-flight test conductor, monitoring systems and adjusting all experimental parameters. The open switch in the safety pilot's control

path indicates that he keeps his hands and feet off the controls during the evaluation runs, assuming control between data-gathering runs and in emergencies. He has several electrical and hydraulic mechanisms for disengaging the Micro-DFCS and the variable-response system in the event of a malfunction, as well as an "automatic go-around" abort mode which makes safe experimentation through touchdown possible. The abort mode commands a 20° flap setting and climb power when activated; at 70-knots (36 m/s) airspeed on a 6° glideslope, an up-flap "hardover" failure can be corrected and climbout can be initiated with a maximum altitude loss of 10 ft (3 m).

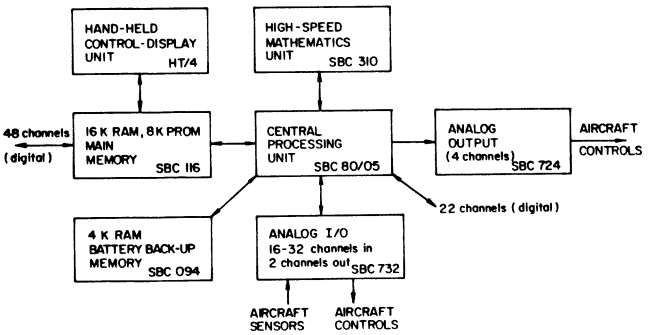


Fig. 3. Microprocessor digital flight control system (Micro-DFCS), model 1.

Microprocessor Digital Flight Control System (Micro-DFCS)

Because the VRA has several levels of backup control (including mechanical direct) and the unaugmented vehicle dynamics provide satisfactory flying qualities, the flight control computer unit (FCCU) of the Micro-DFCS need not be assembled from ruggedized or special purpose components. The FCCU is mounted on a shock-isolated pallet behind the crew in the VRA cockpit, a relatively benign enviornment which allows commercially available microcomputer components to be used for flight control research.

Prior to contract initiation, FRL project members spent several months reviewing currently available microcomputer systems and components. A number of factors were considered in equipment selection, including basic "hardware" characteristics, available software, manipulation bit length, mean cycle time, compatibility with ground-based equipment, program interrupt structure, multiple central processing unit (CPU) option, available analog-to-digital (A/D) and digital-to-analog (D/A) cards, power requirements, data bus structure, and cost. Eleven systems were considered initially; preliminary screening reduced this number to five, and detailed screening reduced the competitors to three. After formal price quotations were obtained, the decision was made to base the Micro-DFCS FCCU on Intel SBC 80/System 80 components.

As shown in Fig. 3, the Micro-DFCS is built around the SBC 80/05 central processing board. This is supported by a high-speed mathematics unit, random-access and programmable read-only memory, A/D-D/A conversion boards, and a hand-held control display unit (CDU). The 8-bit 8085 CPU has a 2-μs instruction cycle time; the CPU board has 22 parallel input/output (I/O) lines, 4 interrupt levels, and a timer, and it operates as the data bus control unit. The mathematics board performs fixed- and floating-point functions; only the latter are used in the initial flight control program, which is called CAS-1. Maximum execution times for 32-bit floating-point add and multiply are 75 and 100 μs, respectively.

The Model 1 Micro-DFCS contains a total of 30.5 K bytes of memory located on the main memory board, the battery backup board, and the CPU board. The CAS-1 program can be contained entirely on the battery backup board, a feature which is used to good advantage in early software development, as discussed below. The main memory board provides communications with the CDU for in-flight monitoring and program control, and it possesses an additional 48 parallel I/O lines.

A/D and D/A conversions have 12-bit resolution. The combination I/O board has a "throughput" rate of 28 kHz and several I/O voltage options; it accommodates 16 differential or 32 single-ended inputs and provides 2 analog outputs. An additional 4-channel output board is included to allow the Micro-DFCS to command the VRA's 6 primary control effectors. The Termiflex HT/4 hand-held control display unit provides double-stroke (keypad plus shift key) input and 2-line, 12-character light-emitting diode (LED) display of ASCII characters. It is functionally equivalent to a conventional 1200-bd keyboard/display terminal, although its display is limited, and multiple key strokes are required to enter most characters.

The FCCU is housed in an RF-shielded, shock-mounted aluminum box. The 6 computer boards identified in Fig. 3 plug into two 4-board cardcages, which allow the addition of two boards to the Micro-DECS without hardware modification. FCCU power ($\pm 5v$, $\pm 12v$) is obtained by regulating the VRA's primary 28 vdc.

Software Development System

The flight control computer unit and control display unit are shown with components of the software development system in Fig. 4. The FCCU and CDU are at the upper left, resting on the ground chassis and power supply used during software development. The keyboard/CRT terminal, acoustic coupler, and telephone extension serve multiple purposes in software development. The terminal provides direct communication with the Micro-DFCS for rudimentary text editing and system monitoring and control. Through the acoustic link to Princeton University's time-shared computer, the terminal is used for primary software development. The IBM 370/158 computer allows more sophisticated text editing, cross-

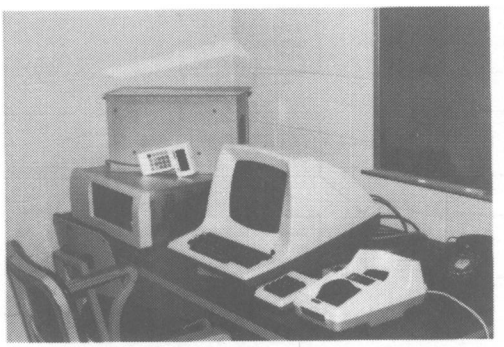


Fig. 4. Components of the Micro-DFCS and software development system.

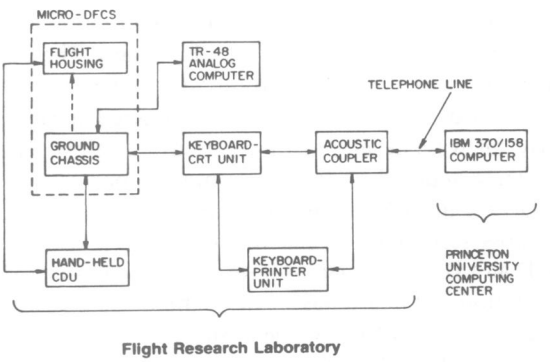


Fig. 5. Equipment layout for Micro-DFCS development.

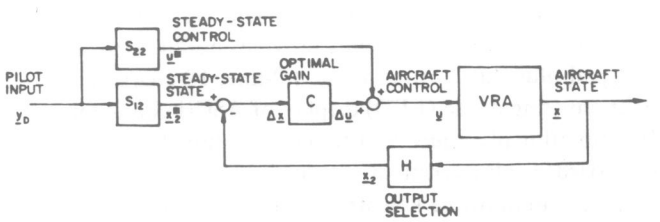


Fig. 6. CAS-1 flight control law. (Underlined symbols correspond to boldface symbols in the text.)

assembly of Micro-DFCS code, and permanent storage of all data files associated with Micro-DFCS software development. The terminal facilitates the direct transfer of data between the Micro-DFCS and IBM computers. Larger flight control programs will be stored in programmable read-only memory (EPROM) during future programs, but CAS-1 can be contained within the 4 K battery backup random-access memory (RAM). (The RAM is volatile, i.e., information is lost when power is shut down. A battery mounted on the RAM board provides the power to save this information for 96 h after external power is turned off.) For initial flight tests, this board is mounted in the ground chassis, and its memory is loaded directly by the University computer. Then the board is removed and installed in the FCCU to complete the data transfer.

Fig. 5 illustrates the relationship between these and other development system components. Not shown in the earlier figure, the keyboard/printer terminal can be used in place of the keyboard/CRT unit for communication with either computer. Prior to flight test, flight control coding is examined in hybrid simulation of the VRA/Micro-DFCS combination. The VRA's dynamic equations are implemented on an EAI TR-48 analog computer, allowing a "real-time" simulation of Micro-DFCS performance to be generated prior to flight.

Experimental Facilities

The VRA is operated from the flight test facility at Princeton University's James Forrestal Campus. The facility includes the FRL hangar, laboratories, and shops, plus a 3000-ft basic utility II runway. A pulse duration modulation (PDM) telemetry system provides 42 data channels, each sampled at a rate of 20/s. TALAR 3 and 4 fixed-beam microwave landing systems (MLS) furnish precision approach-path guidance. The MLS currently are used in a manual mode, driving a cross-needle display which is tracked by the pilot. Fully automatic landings could be investigated by coupling the MLS to the Micro-DFCS. FRL's navy mirror visual approach landing system also is available for investigating carrier approach with a digital flight control system.

CAS-1 Flight Control Development

Control Laws

The first flight control program to be implemented with the Micro-DFCS is a multimode longitudinal command augmentation system entitled CAS-1. It is a "Type 0" linear-optimal controller with a single pilot input (longitudinal stick motion) and a single control output (elevator displacement). CAS-1 has three command modes: direct command, pitch rate command, and normal acceleration command. The direct mode uses no feedback; it simply provides variable stick gearing and a sampled control output (with zero-order hold). The pitch rate mode treats the pilot's longitudinal stick inputs as desired (i.e., command) values of pitch rate (q), and it uses pitch rate and angle-of-attack (α) feedback. The normal acceleration mode interprets pilot inputs as desired values of normal acceleration (n_z), and it uses pitch rate and normal acceleration feedback.

Both digital command augmentation laws can be described by the vector-matrix block diagram shown in Fig. 6. They are designed using "direct digital synthesis," i.e., without first designing equivalent analog systems. Following the nomenclature of [11], these sampled-data control laws can be expressed as

$$\begin{aligned}\mathbf{u}_k &= \mathbf{u}_k^* - CH(\mathbf{x}_k - \mathbf{x}_k^*) \\ &= S_{22}\mathbf{y}_{D_k} + C(S_{12}\mathbf{y}_{D_k} - H\mathbf{x}_k) \\ &= (S_{22} + CS_{12})\mathbf{y}_{D_k} - CH\mathbf{x}_k \end{aligned} \quad (1)$$

where $(\cdot)_k$ denotes the kth sampling instant. Steady-state values of the state and control, $\mathbf{x}$ and $\mathbf{u}$, which correspond to the pilot command $\mathbf{y}_D$ are denoted by $(\cdot)^*$ and are computed from $\mathbf{y}_D$ using the matrices S_{12} and S_{22}. (Formation of these matrices is discussed in [4].) C is the sampled-data regulator gain matrix which is obtained by minimizing a quadratic "cost" function of the state and control, and H is an output matrix which selects the components of the vehicle's motion to be fed back. CAS-1 is designed with a reduced-order model of VRA dynamics. The conventional longitudinal model contains four state variables: velocity (V), flight path angle (γ), pitch rate, and angle of attack. The CAS-1 design model contains only q and α; hence, its gains account for short period dynamics but ignore the phugoid mode.

While both control laws are described by Fig. 6 and [1], the values of S_{12}, S_{22}, C, and H are different, to account for the two interpretations given to pilot commands. For the CAS-1 pitch rate mode, (1) reduces to

$$\delta E_k = c_1 q_{D_k} - c_2 q_{M_k} - c_3 \alpha_{M_k} \tag{2}$$

and the normal acceleration mode reduces to

$$\delta E_k = c_1 n_{z_{D_k}} - c_2 q_{M_k} - c_3 n_{z_{M_k}} \tag{3}$$

where $(\cdot)_M$ signifies a measured value and δE is the elevator command. Comparing (2) and (3) with (1), it can be seen that the leading gains (c_1) each serve three functions. Given a constant pilot input, c_1 scales the input to provide an elevator increment that includes the steady-state elevator setting and accounts for the desired steady-state values of the two feedback variables. The remaining gains modify the aircraft's closed-loop dynamics to yield, for example, the desired step response rise time and overshoot.

Examples of these gains and the resulting step responses (obtained from all-digital simulation with a sampling rate of 10/s) are presented in Table II. Angles are measured in radians and normal acceleration is expressed in g's. Direct mode responses assume a step elevator input, while the CAS modes are based on pilot step commands. Pitch rate mode A weights q more heavily in the design cost function than mode B does. All three cases provide quickened response and improved damping. Since positive α causes positive n_z, the sign of c_3 is reversed for the two CAS modes.

TABLE II
CAS-1 Gains and Predicted Step-Response Characteristics (IAS = 105 kt)

Mode	Gains			Step Response	
	c_1	c_2	c_3	Rise Time (s)	Overshoot (percent)
Direct (pitch rate)	-	-	-	0.19	47.5
Direct (normal acceleration	-	-	-	0.7	10.8
Pitch rate (A)	−0.89	−0.62	0.47	0.11	1.
Pitch rate (B)	−0.77	−0.43	0.32	0.14	6.5
Normal acceleration	−0.37	−0.53	*−0.18*	*0.35*	*3.4*

TABLE III
CAS-1 Program Table of Contents

1. Executive Routines
   - 1.1 Initialization
   - 1.2 Error Detection
   - 1.3 CDU Interface
   - 1.4 Keyboard Command Recognition
2. Flight Control Routines
   - 2.1 Direct Mode
   - 2.2 Pitch Rate Command Mode
   - 2.3 Normal Acceleration Command Mode
3. Utility Routines
   - 3.1 Count-up Display
   - 3.2 Hexadecimal-to-Decimal Conversion
   - 3.3 Mathematics Unit Driver
   - 3.4 Analog-to-Digital Conversion
   - 3.5 Mode Change Routine
   - 3.6 Calibrated Step Input
   - 3.7 Block Data Moves
   - 3.8 Block Memory Erase
   - 3.9 Numeric Keyboard Input

Software

The CAS-1 program occupies approximately 2.5 K of Micro-DFCS storage in its present form. At the nominal sampling rate of 10/s, the execution duty cycle requires 6 percent of the time available. The coding is efficient but not fully optimized, so there is substantial room for growth in future flight control programs.

The major elements of CAS-1, arranged in chapter format, are listed in Table III.

The error detection routine checks the contents of memory every 5 s, checks for mathematical errors on every operation, and flashes a light on the safety pilot's panel when a flight control routine is being executed. The flight control routines are initiated by a timed interrupt. The sampling interval and gains can be modified in flight, and up to 20 separate flight control modes can be addressed by the current CAS-1 assembly. The flight control routines account for known sensor biases, provide proper scaling of outputs, and limit outputs to prevent D/A overflow. The count-up display routine generates an increasing sequence of numbers (reset each 10 s) which indicates that the timed interrupt is working, the program has initialized correctly, and the D/A channels and executive routine are operational. The numbers are displayed on the CDU and sent to the ground via telemetry. The calibrated step input routine allows the pilot to enter a step input on any one of the analog input lines. After keying in the desired voltage, the input is initiated by depressing the CDU's "carriage return" key. The step input is nulled by depressing any CDU key.

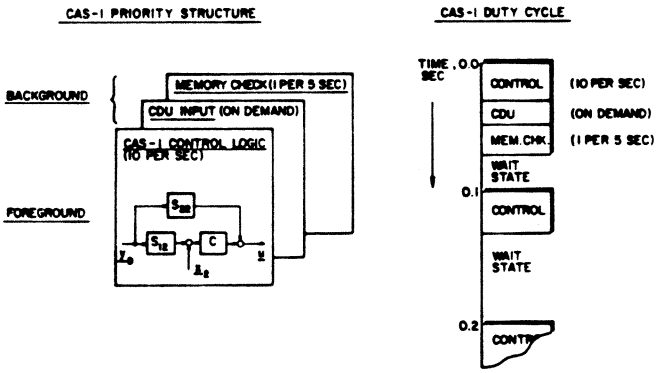


Fig. 7. CAS-1 program organization.

TABLE IV
Micro-DFCS Analog Inputs and Outputs

Inputs			
1.	Elevator position	9.	Aileron Position
2.	Throttle position	10.	Rudder position
3.	Direct lift flap position	11.	Side-force panel position
4.	Angle of attack	12.	Sideslip angle
5.	Pitch angle	13.	Roll angle
6.	Pitch rate	14.	Roll rate
7.	Airspeed	15.	Yaw rate
8.	Normal acceleration	16.	Lateral acceleration
Outputs			
1.	Elevator command	4.	Aileron command
2.	Throttle command	5.	Rudder command
3.	Flap command	6.	Side-force panel command

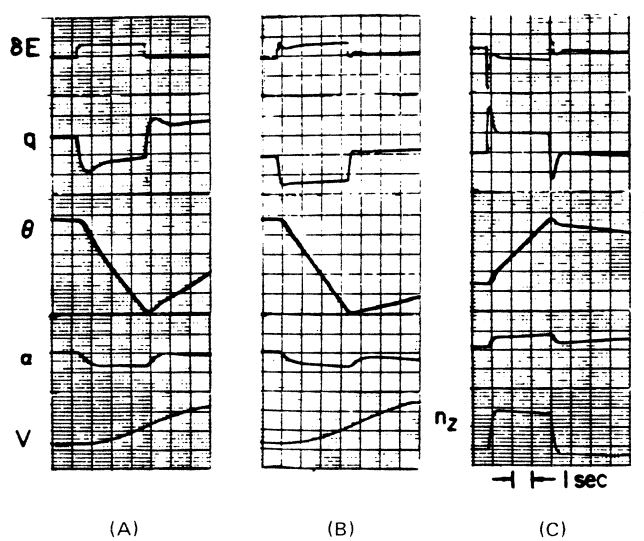


Fig. 8. Hybrid Simulation results for three CAS-1 command modes. (A) Direct mode. (B) Pitch rate mode (B). (C) Normal acceleration.

Two alternative descriptions of the CAS-1 program are shown in Fig. 7. The flight control routine operates with highest priority (in the "foreground"), and all other routines are executed in the remaining available time (in the "background"). The resulting duty cycle also is shown in the figure.

The first 16 analog input signals and 6 analog output signals have been defined for use by CAS-1 and the expanded programs which will follow. They are described in Table IV.

Hybrid Simulation Results

As mentioned previously, CAS-1 performance can be investigated prior to flight by operating the Micro-DFCS in conjunction with a fourth-order analog simulation of the VRA. Examples of simulation results are shown in Fig. 8, which is a direct copy of the analog computer's strip chart output. The step inputs for Figs. 8(A) and 8(B) were generated manually, while the calibrated step input was used in Fig. 8(C).

The direct mode [Fig. 8(A)] demonstrates the predicted open-loop response of the system. Because the "step" input has a finite rate, the D/A converter picks up an intermediate value prior to reaching the final value; the elevator input is "staircased" as a consequence. Pitch rate is seen to overshoot and decay, α reaches a new steady state, and velocity increases as the aircraft begins to dive. When the stick is released, α returns to its original value; the increased velocity leads to a positive pitch rate and a rapid pitch angle (θ) increase.

The pitch rate mode [Fig. 8(B)] shapes the elevator input, providing quicker q response with less overshoot. The q decay is reduced but not eliminated, as reduced-state feedback is used and the control law is not "Type 1." [A Type 1 control system contains one pure integration in series with each control actuator. It can achieve zero steady-state error if properly designed [12].] Upon releasing the stick, q returns to a smaller value than in the previous case, and the rate of θ increase is reduced.

The normal acceleration mode [Fig. 8(C)] forces a large q overshoot to obtain rapid, well-damped n_z overshoots its original value but α remains above its original value. Decay in θ is slower than in the previous two cases, and adjustment to the initial conditions progresses on the time scale of the phugoid mode.

Flight Test Results

The first flight test of the Micro-DFCS in the VRA was conducted on June 28, 1978. Telemetry records were not obtained, but the flight test crew obtained useful qualitative information on each of the command modes.

Direct mode response and response of the conventional mechanical system are virtually identical for normal maneuvering inputs and 10/s sampling rate.

Although the discrete control signal takes the form of a sequence of step inputs, the control jumps are perceptible only when control motions are large and rapid. Reducing the sampling rate to 8/s makes the control jumps more obvious but does not degrade the VRA's flying qualities. In both cases, the pilot's perception of the control jumps is based on sound rather than vibration or rigid-body motion of the aircraft.

Both pitch rate modes A and B (plus two others) were found to provide smooth control with no perceptible sampling effects, even for large calibrated step inputs. D/A overflow protection involved low stick gearing which, in turn, made it impossible to distinguish between the flying qualities of the four sets of pitch rate mode gains. A software modification will eliminate this problem.

The normal acceleration mode proved to be too sensitive to structural vibration, as presently coded in CAS-1. The VRA control system monitors the difference between commanded and actual elevator position, and it disengages the actuator when this error becomes too large. Vibrations sensed by the accelerometer led to elevator commands which tripped this "fail-safe" mechanism, preventing flying qualities evaluation of the mode on the first flight. Appropriate filtering will be added for future flights.

Future test flights will examine the subjective characteristics of the CAS-1 command modes and produce quantitative measures of closed-loop dynamic characteristics. Various sampling rates will be examined, and limiting values of system parameters will be defined.

Future Flight Control Programs

The CAS-1 program is intended as a first step in digital flight control research, and it will be superseded by a series of programs with increasing complexity and capability. Table V summarizes the current plans for six Micro-DFCS programs leading up to a fully coupled digital flight control system. The thrust of this effort is directed at control laws, but state estimation and on-line parameter identification will be addressed when there is indication that they will contribute to improved flying qualities or enhanced control system performance.

Parallel efforts in these and other areas, e.g., redundancy management, fault detection and correction (including "analytical redundancy"), and closed-loop navigation and guidance, also are contemplated, although they are not included in the current program.

TABLE V
Future Flight Control Programs

CAS-2: Full longitudinal control (conventional)
- Angle-plus-velocity command augmentation system
- "Type 0" with rate restraint and "Type 1" structures
- Two pilot inputs (longitudinal stick and throttle lever)
- Two aircraft controls (elevator and throttle setting)
- Four-state feedback

CAS-3: Initial lateral-directional control
- Separate "Type 0" roll and yaw command augmentation systems
- Each control law has:
  - Single pilot input
  - Single aircraft control
  - Two-state feedback

CAS-4: Full lateral-directional control (conventional)
- Integrated roll-yaw command augmentation system
- "Type 0" with rate restraint and "Type 1" structures
- Two pilot inputs, two aircraft controls, and four-state feedback

CAS-5: Integrated direct lift control
- CAS-2 plus DLC

CAS-6: Integrated direct side-force control
- CAS-4 plus DSFC

CAS-7: Fully coupled command augmentation
- CAS-5 plus CAS-6
- Cross-axis coupling
- Gain scheduling

Plus:
- State estimation
- Parameter identification

Conclusion

The promise which digital computation holds for future flight control systems is that powerful new theoretical concepts can be reduced to practice and used to improve the safety, reliability, and effectiveness of aircraft operations. Flight testing new concepts at an early stage of development can aid this transfer of technology. The VRA/Micro-DFCS program at Princeton University is providing a focus for digital flight control development by combining research on control theory and microprocessors with flight experimentation.

Acknowledgment

James C. Seat, Second Lieutenant, USAF, is conducting graduate research on digital flight control and has had a major responsibility for the results discussed here. George E. Miller, member of the FRL technical staff, has been responsible for systems installation and checkout, as well as flight test operations.

References

[1] P.R. Motyka, E.G. Rynaski, and P.A. Reynolds, "Theory and flight verification of the TIFS model-following system," *J. Aircraft,* vol. 9, pp. 347-353, May 1972.

[2] J.T. Gallagher, I. Saworotnow, R. Seeman, and T. Gossett, "A model-following variable stability system for the NASA ARC X-14B," *J. Aircraft,* vol. 9, pp. 461-469, July 1972.

[3] G. Stein, G.L. Hartmann, and R.C. Hendrick, "Adaptive control laws for F-8 flight test," *IEEE Trans. Automat. Contr.,* vol. AC-22, pp. 758-767, Oct. 1977.

[4] R.F. Stengel, J.R. Broussard, and P.W. Berry, "Digital controllers for VTOL aircraft," *IEEE Trans. Aerosp. Electron. Syst.* vol. AES-14, pp. 54-63. Jan. 1978.

[5] H.N. Tobie, and K.W. Ramby, "A practical solution to automatic landings using digital flight control computers," AIAA Paper 70-1032, Aug. 1970.

[6] M.A. Mathews, Jr., "SAAB digital flight control," AIAA Paper 74-76. Jan. 1974.

[7] S.S. Osder, D.C. Mossman, and B.T. Devlin, "Flight test of a digital guidance and control system in a DC-10 aircraft," AIAA Paper 75-567, Apr. 1975.

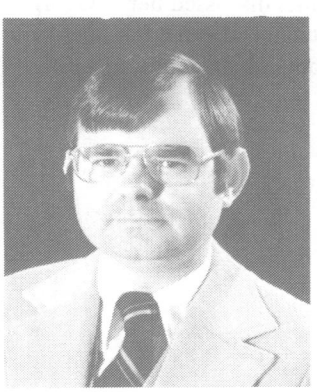
[8] T.R. Yechout, D.R. Oelschlaeger, "Digitac multimode flight control system," AIAA Paper 75-1085, Aug. 1975.

[9] R.K. Smyth, "Avionics and controls state of the art survey (SOAS)," presented at the NASA Workshop on Avionics and Controls Research and Technology, Hampton, Va., June 1978.

]10] J.L. Lockenour, and G.P. Layton, "RPRV research focus on HiMAT," *Astronaut. Aeronaut.,* vol. 14, pp. 36-41, Apr. 1976.

[11] R.F. Stengel, J.R. Broussard, and P.W. Berry, "Command augmentation control laws for maneuvering aircraft," AIAA Paper 77-1044, Aug. 1977.

[12] N. Sandell, Jr., and M. Athans, "On type-L multivariable linear systems," *Automatica,* vol. 9, pp. 131-136, Jan. 1973.



Robert F. Stengel (M'77) received the B.S. degree in aeronautics and astronautics from Massachusetts Institute of Technology, Cambridge, and the M.S.E., M.A., and Ph.D. degrees in aerospace and mechanical sciences from Princeton University, Princeton, N.J.

He is currently Associate Professor of Mechanical and Aerospace Engineering and Director of the Flight Research Laboratory at Princeton University. His current research deals with aircraft dynamics, control, and parameter identification. Previously, he headed the Vehicle Controls Section at The Analytic Sciences Corporation, where he studied aircraft stability and control during extreme maneuvering, aircraft fuel conservation, digital control of helicopters, and dynamics of the human pilot. He contributed to the digital flight control systems of the Apollo Lunar Module and the Space Shuttle while a group leader at the Charles Stark Draper Laboratory, and he was an aerospace technologist at NASA Wallops Station. He holds a patent for a wind velocity probing device and has published over two dozen technical papers.

Dr. Stengel is an associate fellow of the American Institute of Aeronautics and Astronautics and a member of the IEEE.