Lecture/Laboratory #13

- Lab Review
- Lecture Review

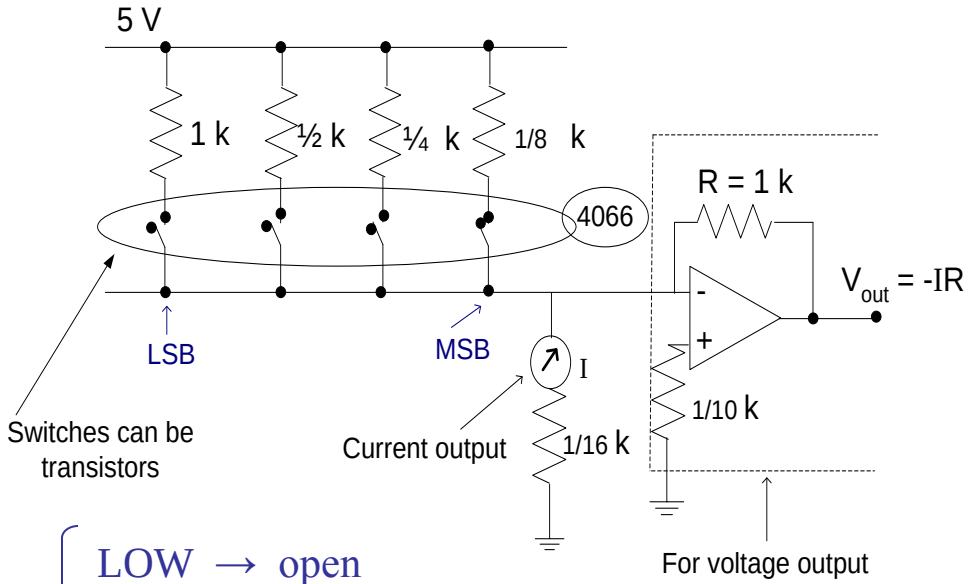
- D/A and A/D converters
- Converter Errors
- Timing with Counters
- Latches and Registers
- Start of Digital Sampling Oscilloscope (Front end)

Lab ⇒ Connect A/DC with D/AC

Analog signal input → look for analog signal output (for restoration of analog signal accuracy)

Connect output of A/DC to LED and observe flashing

Digital – to – Analog Conversion



Input { LOW → open
HIGH → closed

16 possible current (voltage) values depending upon which switches are closed.

R = 1 k → 2^0 (= 1)

R = ½ k → 2^1 (= 2)

R = ¼ k → 2^2 (= 4)

R = 1/8 k → 2^3 (= 8)

Op-amp for voltage output.

For 12 – bit system range of resistor values 2000:1! Other solutions, which may not require such large range of resistors with precision determined by the smallest one.

Analog – to – Digital Conversion

A/DCs are available commercially as ICs (chips)

Number of different A/D converters

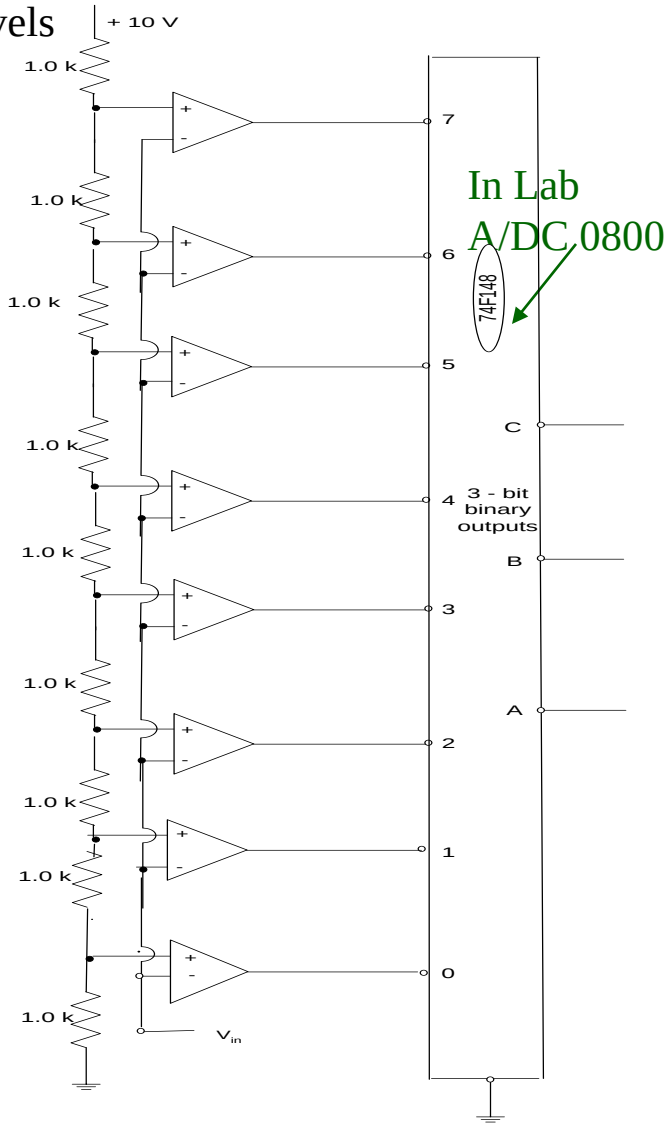
Parallel – encoded ("flash") A/DC

It is the fastest method of A/D conversion. The delay time from input to output = comparator + encoder delays.

Commercial : 16 to 1024 levels

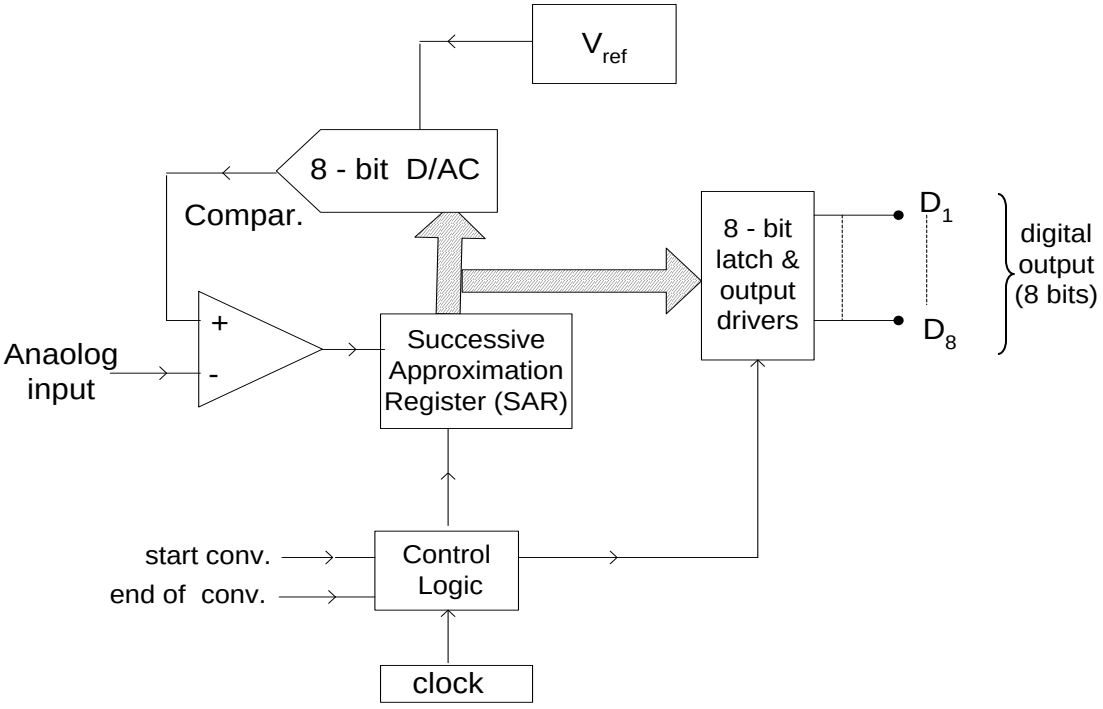
(4 – bit to 10 – bit outputs).

Input V_{in} is fed simultaneously to one input of N comparators. Other inputs are connected to N equally space refer. Voltages. Encoder generates a digital output ~ to highest comparator by V_{in}.



A/DC – Successive Approximation

Output codes (digital) are feed – in into D/AC and are compared with analog input via a comparator.

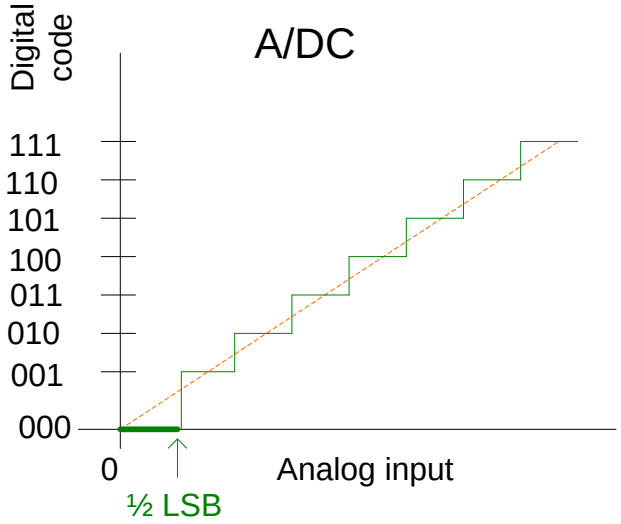


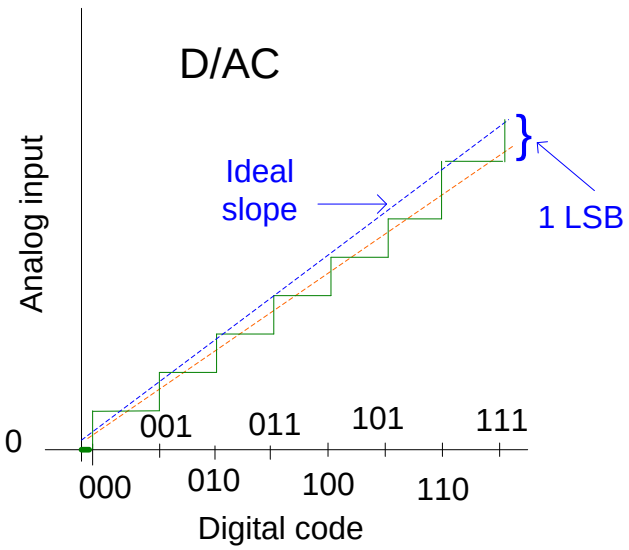
Start: all bits = 0 : MSB $\Rightarrow$ 1 and following bits $\Rightarrow$ 1. If D/AC output does not exceed the input voltage, this bit stays 1. Otherwise, it is set 0. For N – bit A/DC , N-such steps are required. Successive approx. A/DC has begin conversion ("start") input and conversion done ("end") output. Digital output $\Rightarrow$ parallel format.

Converter Errors

Errors related to A/D and D/A converters are in broad range. We will concentrate on the two most comon types of converter errors.

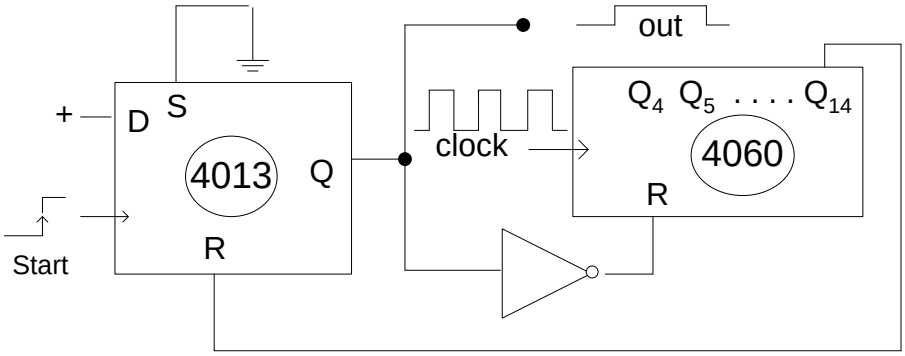
Examples:





Timing with Counters

Flip – flops and counters (cascaded toggling FFs) can be used to generate a long output pulse. IC 4060 is a 14 stage CMOS binary counter (14 cascaded FFs) ⇒ scheme and principle of work:



A rising edge at the input brings Q HIGH → enabling counter. After 2^{n-1} clock pulses (n_{max} for our example is 14) Q_n goes HIGH resetting FF (4013) and the counter, and cycle can start again.

⇒Generation accurate long pulse, which length can be varied by 2 (depending on number of Q_n involved).

The 4060 has internal oscillator, which can eliminate need for external clock.

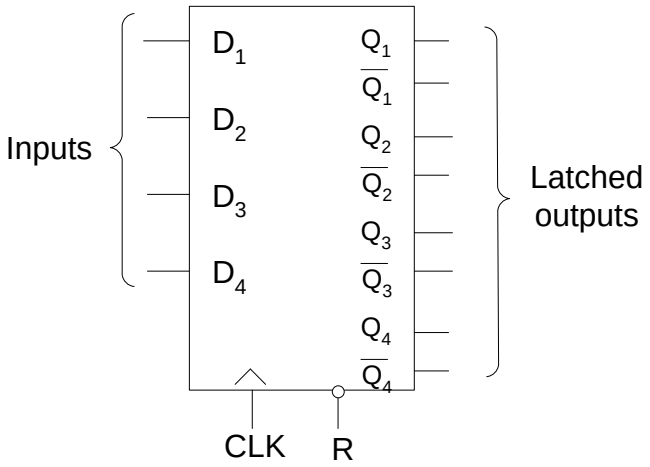
Latches and Registers

Latches and registers → to hold a set of bits even if inputs change.

Register: is a set of FFs

Latch: is a special register ⇒ outputs follow inputs when enabled, and hold the last value when disabled.

74 LS 174 is 4 – bit D register:

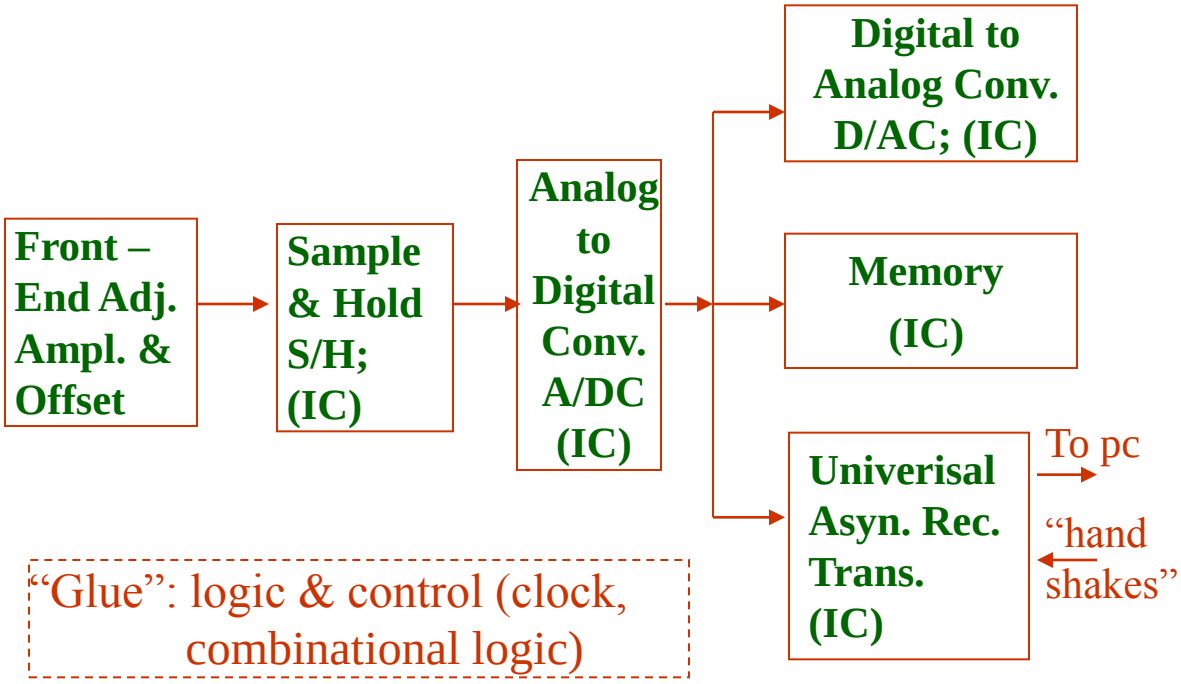


This is quad D register with true (Q) and complemented ($\overline{Q}$) outputs.

Latches and registers are available with three – state outputs (e.g. 4 – bit 8551 D – register), which can be used in data "bus".

Digital Sampling Oscilloscope (DSO)

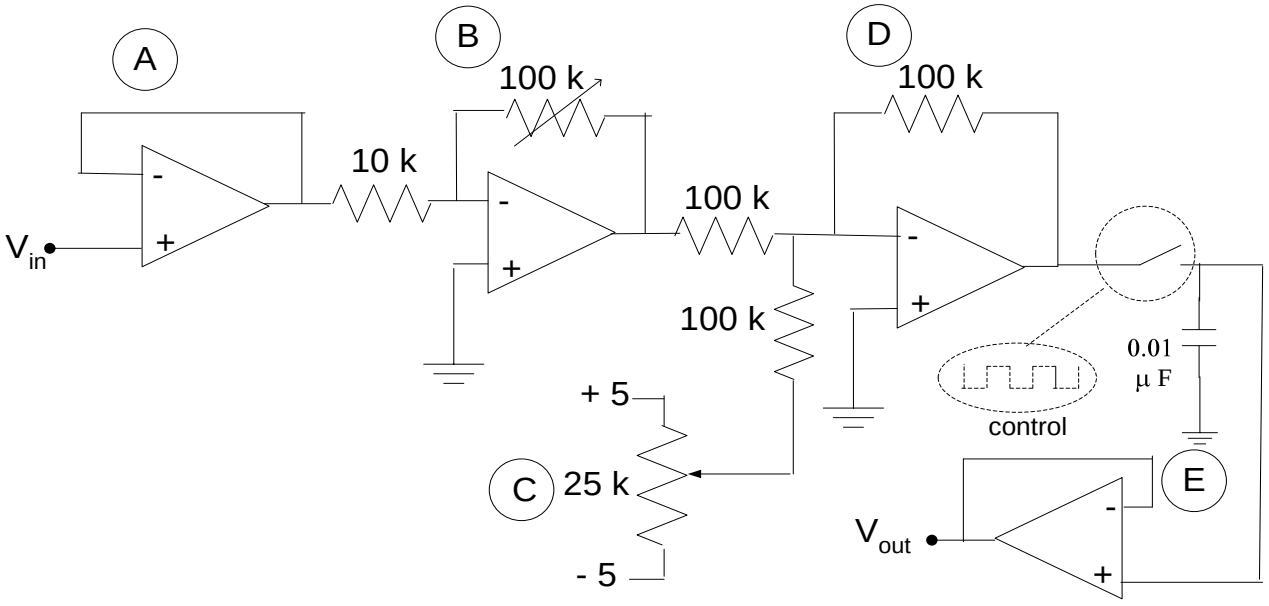
Block diagram:



Modes of Operation ⟹

1. Acquisition Mode (Memory) →Not fast
2. Display Mode (Reading from memory) → Fast
3. Transfer Mode ← Slow

DSO (cont.) Front End (cont.)



A High Z_{input} Voltage follower:

Z_{in} = 2 MΩ , Z_{out} = 75 MΩ

B Variable gain amplifier: Z_{in} = 10 k, Gain = 0 – 10 x

C DC offset adjustment : $I_{in} \pm$ 2 mA (adding voltage follower → better circuit)

D Summing amplifier: Output here is DC adjusted

E Sample – and – hold: C = 0.01μF was selected in order to provide sampling rate at 40 μsec with precision 1:256

$\Rightarrow$ 40 μsec x 256 = 10^{-2} sec

τ = RC = 0.01 μF x 1 MΩ = 10^{-2} sec

Start of Digital Sampling Oscilloscope (DSO)

Specifications:

Inputs: 1 channel (2 channels → by alternating →
(analog) → using 4066)

~ 10^6 Ω impedance

- 5 → + 5 voltage range

0.5 – 20 adjustable gain

-5 → +5 adjustable bias

Outputs

(analog): ~ 100 Ω output impedance

(digital): 1200 bane (= bit/sec) data transfer rate

Sampling and Memory:

~ 100 → 3 kHz adjustable sample rate

~ 2000 bytes RAM (Random Access Memory) capacity

DSO (cont.)

Manual (Report)

→ Display (set up of the board, features)

Table of Contents

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- Channels (range)
- Offset and Gain

→ Operation II (details, “theory”)

→ Conclusions, Improvement Suggestions etc.

→ Figures (Figures can be both inside the text and at the end)

→ Tables

→ Appendix (A, B, C, . . .etc.)