Lecture/Laboratory #9

- Comments/Discussion Laboratory Work
- Review Gates

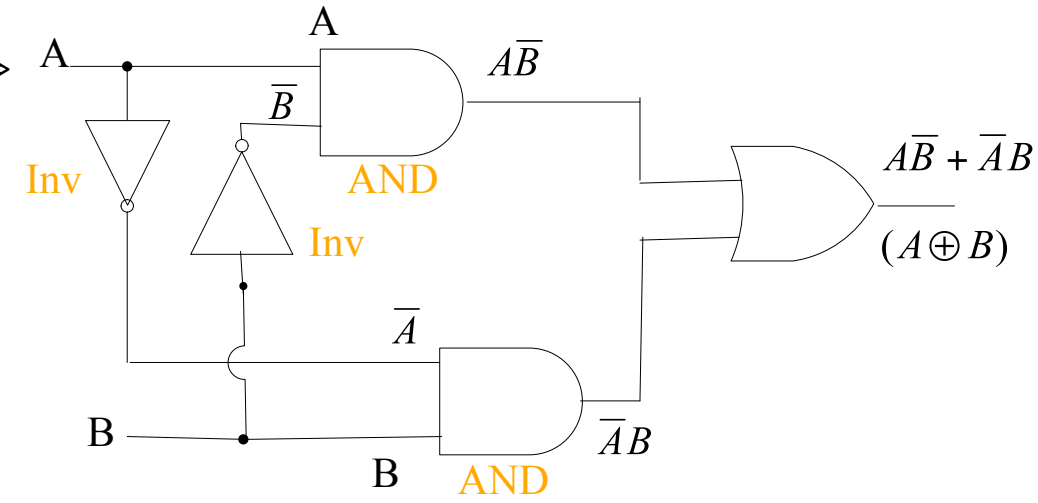
- Logic Identities
- TTL and CMOS Gates (Example)
- Introduction to Three – State and Open – Collector Logics (TRI – State)
- Sequential Logic (Memory)

Logic Identities (Cont.)

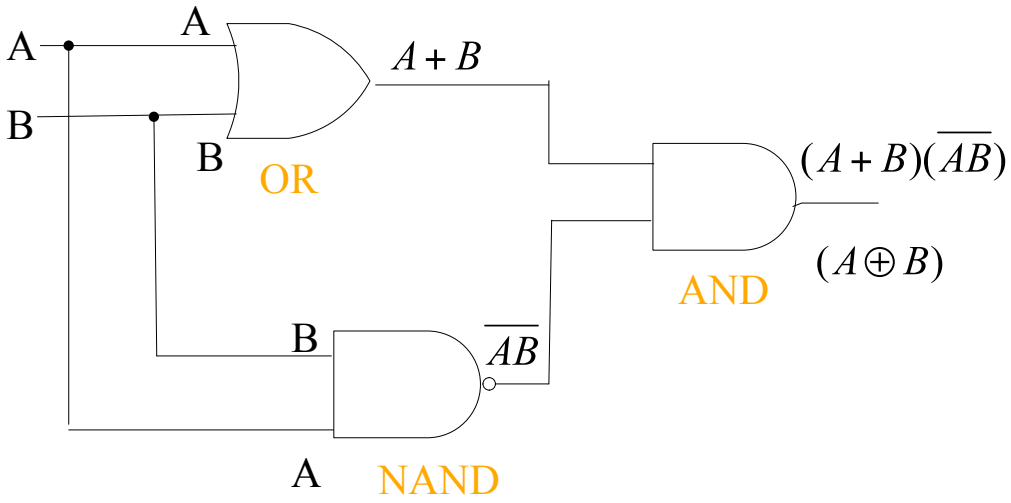
Realization of $A \oplus B = \overline{A}B + A\overline{B}$ and $A \oplus B = (A + B)(\overline{AB})$

(XOR Gate)

$\overline{A}B + A\overline{B} \Rightarrow$



$(A + B)(\overline{AB})$

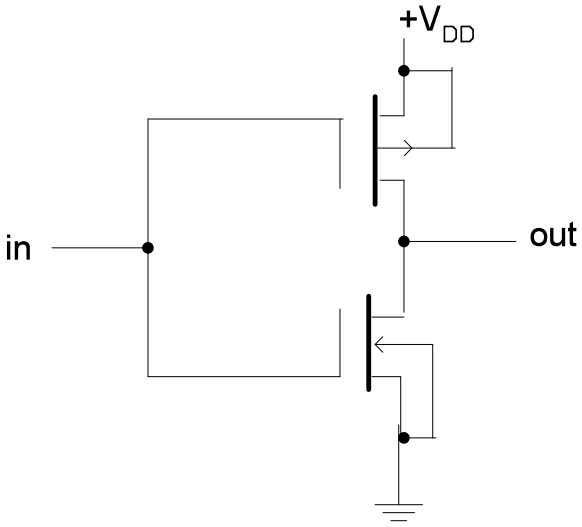


CMOS and TTL

CMOS (complementary MOS) and TTL (transistor – transistor logic) are two most popular logic families in current use. Integrated circuits (IC) → large variety of functions for both types (CMOS and TTL) Large-Scale Integration (LSI) → mostly CMOS (n – channel → NMOS).

These are high-speed logics

Inverters and Gates with CMOS

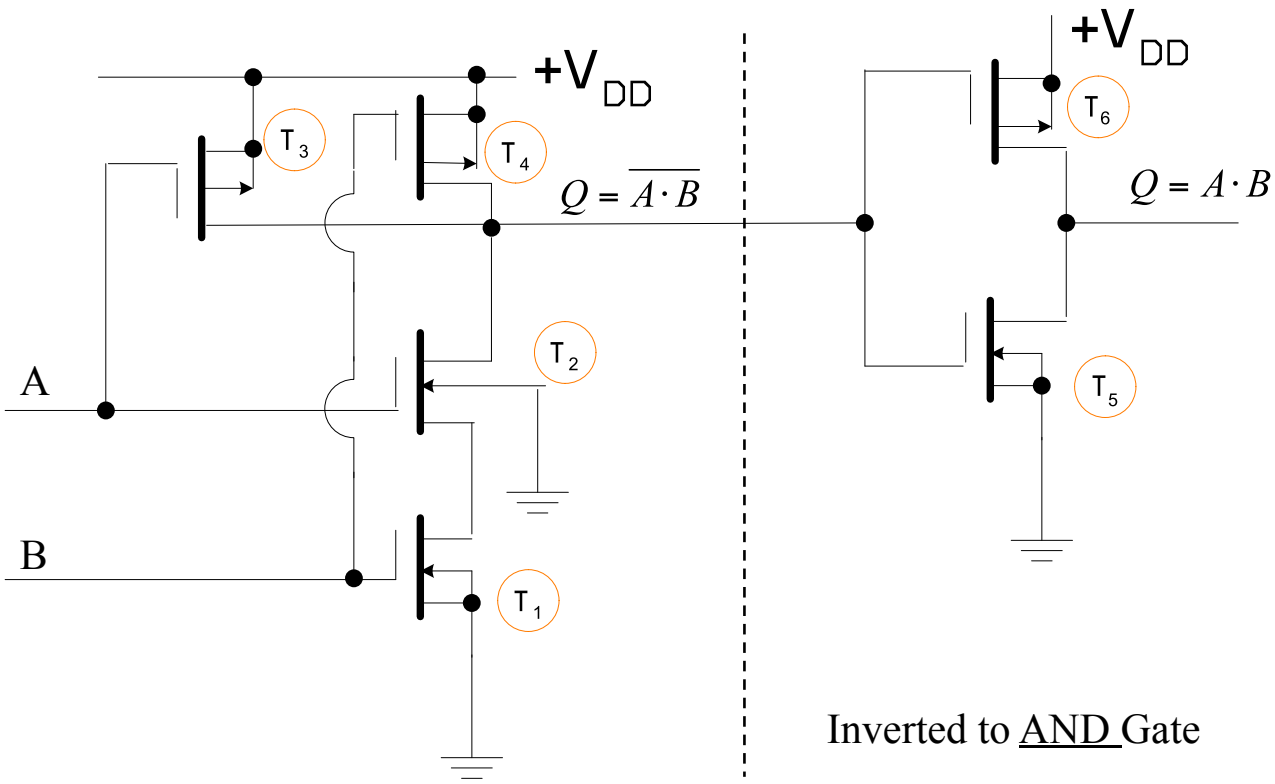


Similar to push-pull switch. Analysis: 0 – input (Low) → bottom transistor "off" and top one "on" pulling output HIGH ($+V_{DD}$). For input HIGH (e.g. $+V_{DD}$) bottom transistor "on" and output pulled to ground (LOW).

CMOS Logic Inverter

Input LOW → output HIGH and vice versa

Inverters and Gates with CMOS (cont.)



CMOS NAND Gate

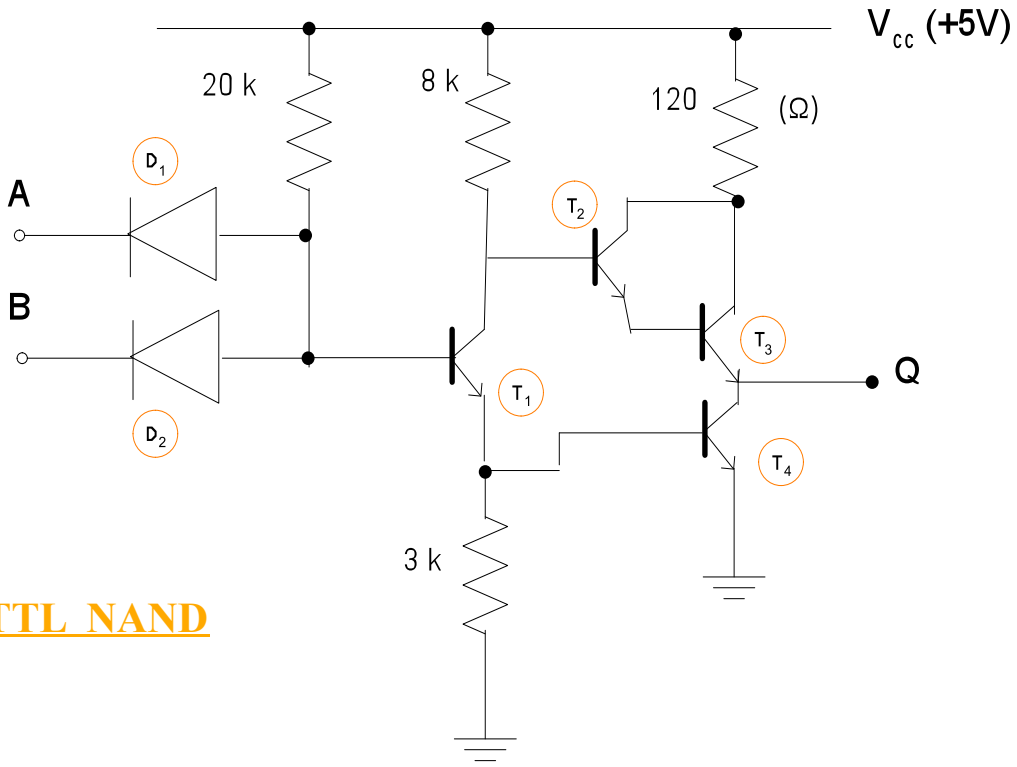
Analysis: (a) If inputs A and B are both HIGH, CMOS transistors T_1 and T_2 (n – channel ⇒ NMOS) are both "ON" and output Q is LOW (near ground while transistors T_3 and T_4 (p – channel ⇒ PMOS) are "OFF" (no current flows). A, B HIGH ⇒ Q LOW

(b) If A or B or both are LOW, T_3 or T_4 or both are ON (while one of T_1, T_2 is "OFF") and output is HIGH ($+V_{DD}$). A or B (or both) LOW ⇒ Q HIGH

Inverters and Gates with TTL

Transistor – transistor Logic (TTL) provides inverters and gates similarly as CMOS, although TTL characteristics are different than CMOS.

Let us consider NAND gate with the bipolar low-power Schottley (LS) TTL:



TTL NAND

Analysis: Inputs A, B on diodes D_1 , D_2 are driving transistor inverter followed by a push-pull output. If A and B are HIGH, the 20 kΩ resistor provides V for T_1 to be "ON",

Inverters and Gates with TTL (cont.)

which provides saturates T_4 and turning "OFF" Darlington pair T_2,T_3, hence output is LOW (zero).

If A or B (or both) are LOW one of Diodes (or both) is conducting providing V = 0 on base of T_1 (T_1 is OFF) and T_4 (T_4 is also OFF). Because T_1 is OFF, base of T_2 (and T_3) is HIGH and Q is HIGH ⇒ LOW for A or B or AB ⇒ HIGH out.

Some characteristics of TTL and CMOS

TTL requires +5V supply; CMOS : +5 - +15 V the most common: +5V, +12V

TTL: to pull it LOW it requires sink the current (usually ~ 1 mA); CMOS has no input current.

Output ⇒ TTL: saturated transistor to ground for LOW and emitter follower for HIGH

Output ⇒ CMOS: MOSFET is turned on to V_{DD} (HIGH) or to ground (LOW)

Speed ⇒ TTL: 25 – 50 MHz; CMOS: slower, but less power dissipated.

Introduction to Three – State and Open – Collector Logic ("TRI – STATE")

In the TTL and CMOS gates the output is held either HIGH or LOW by transistor or MOSFET being "ON". Nearly all digital logic uses this type of circuit, because it provides low output impedance in both states ⇒ faster switching time and better noise immunity in comparison, e.g., with single transistor.

However, such circuits (devices) are unsuitable for systems with several functional units, which have to exchange data (e.g. computer). It would be very unpractical to connect each unit with one another with 16 wire cables (for 16-bit words) in order to send and receive 16 – bit words.

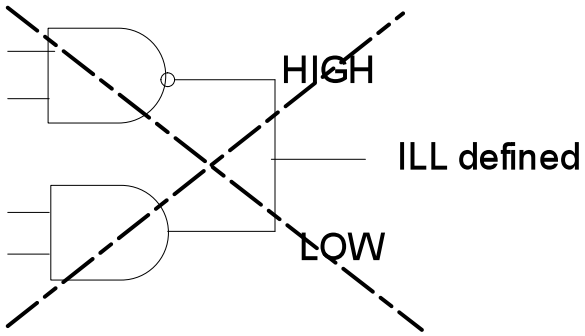
Solution ⇒ data bus: a single set of 16 wires accessible to all devices. Each device can receive data but only one in the time can send the data. Therefore, the bus system requires control device, which decides who may "talk" at given moment ("bus master").

The gates, which we've discussed, cannot be used in its regular form because they have all time two active states (HIGH and LOW). By connecting such gates to the system, they would play all time active role ("talk") due t LOW and HIGH signals. Therefore gates with "open" (no active) output are needed.

Introduction to Three – State and Open – Collector Logic (cont.)

Solution: "three – state" and "open – collector" devices. Such devices (gates) have now three states: LOW, HIGH, and OPEN (open ckt).

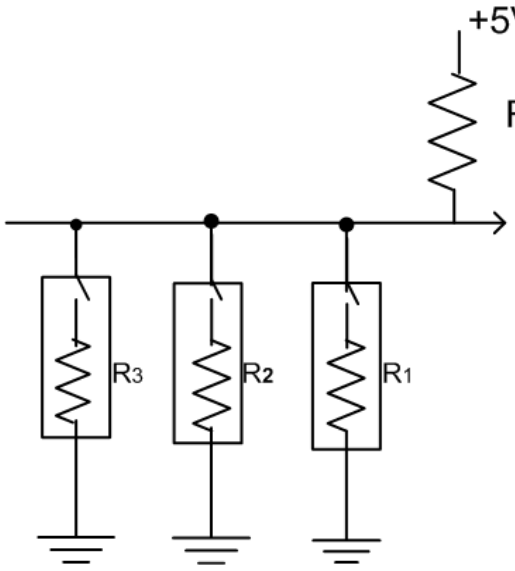
Open – collector gate (similarly three-state) has output without pull-up transistors (see e.g. TTL NAND). Such transistors have to be replaced by pull-up resistor in attached ckt. Value of the resistor is not critical and may range from a few hundred to a few thousand Ω.



Not allowed in TTL

TRI – STATE Logic (cont.)

Pulling structure

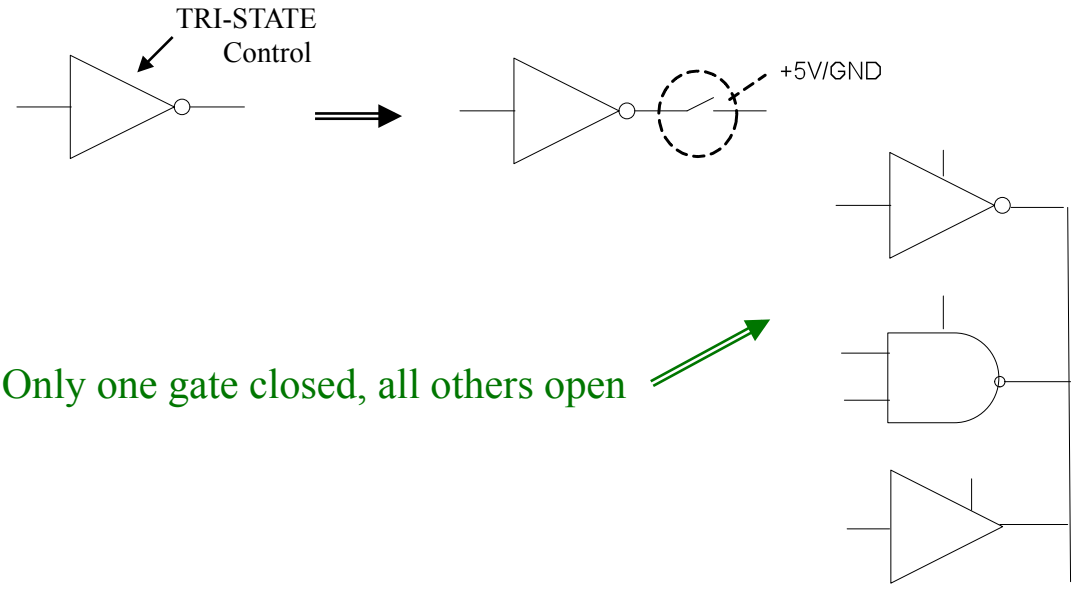


← Pull up

Only can pull LOW
(not HIGH)

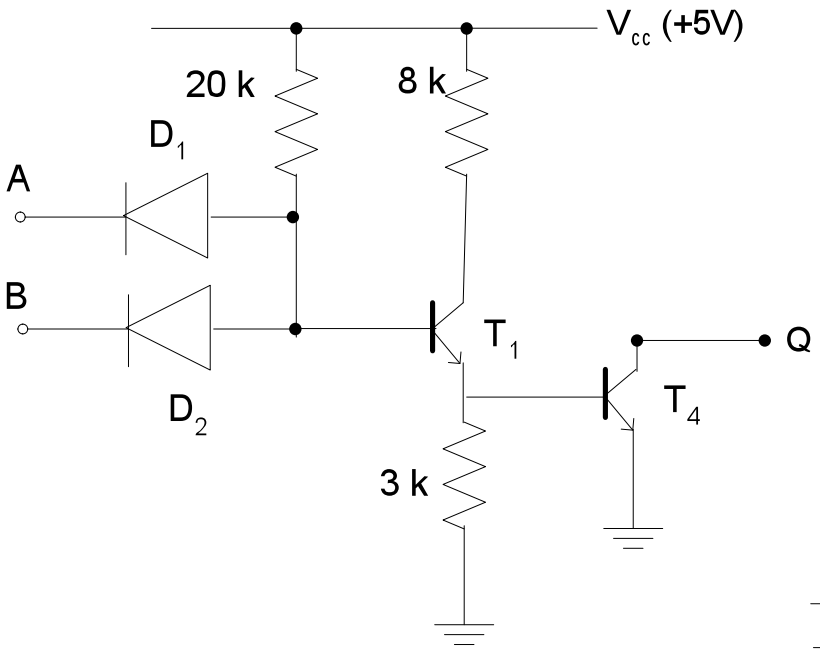
Open – Collector ⇒ doesn't have internal pull up ⇒ No HIGH
only LOW

This allows multiple connection

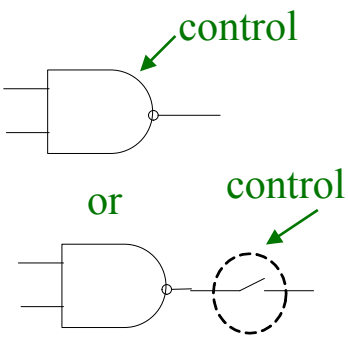


Only one gate closed, all others open

Open-Collector Gates



Equivalent to:



Open – collector NAND

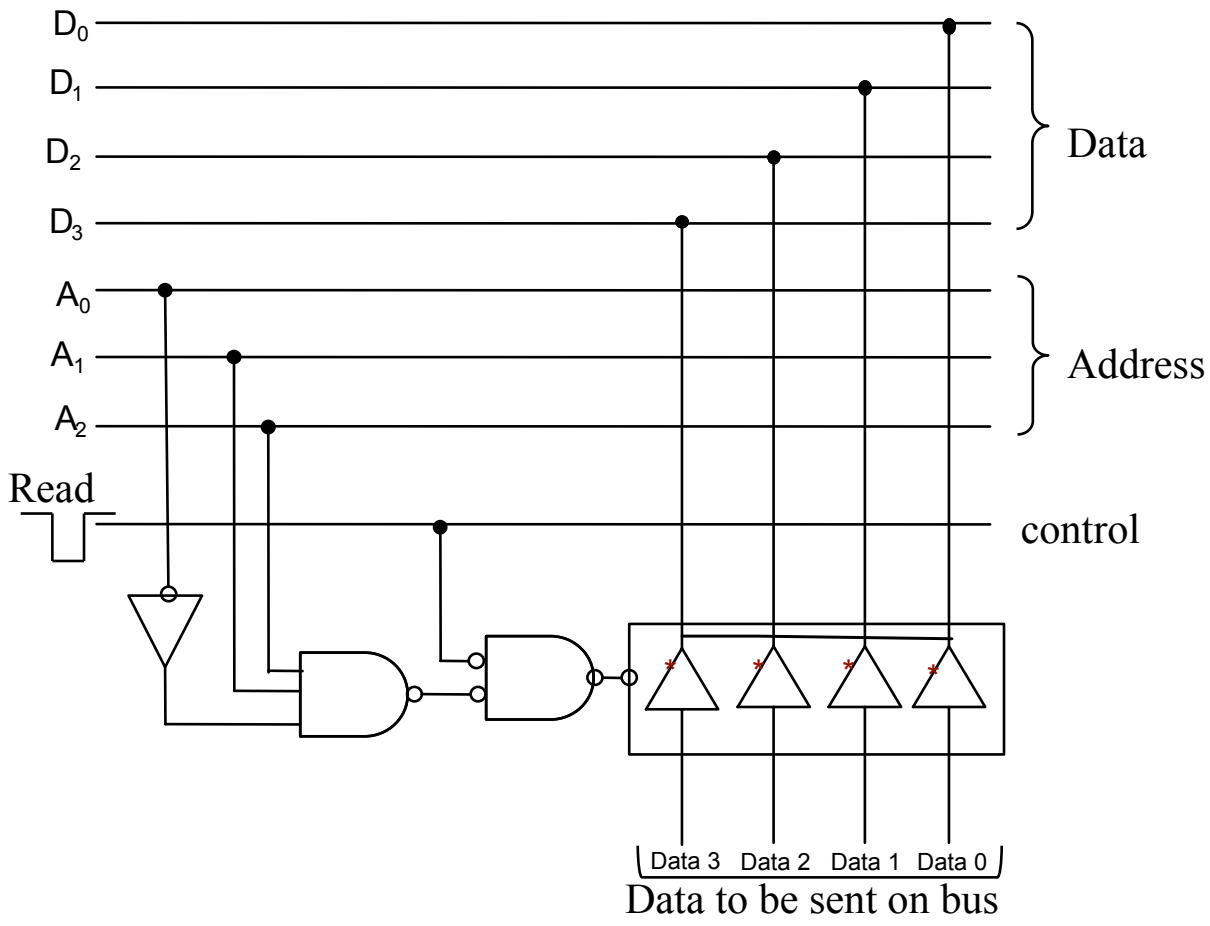
Similarly three – state gates can be built

Example of Application: Data Buses

Open – collector gates (as well as three-state gates) can be used to drive a data bus. Each line of the bus has single pull-up resistor, and every device that needs to put data on the but ties onto it with three-state gates (marked with asterisk).

Example of Application: Data Buses (cont.)

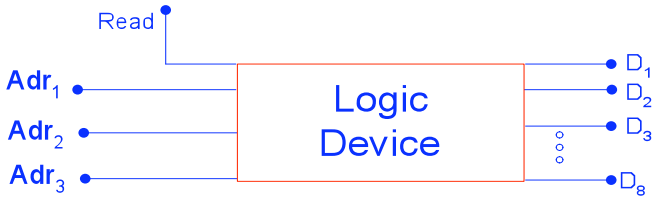
At most one device has its drivers enabled at any instant, and all devices being disabled into open (third) state. The selected device assert data onto the bus by recognizing its particular address on a set of address and control lines.

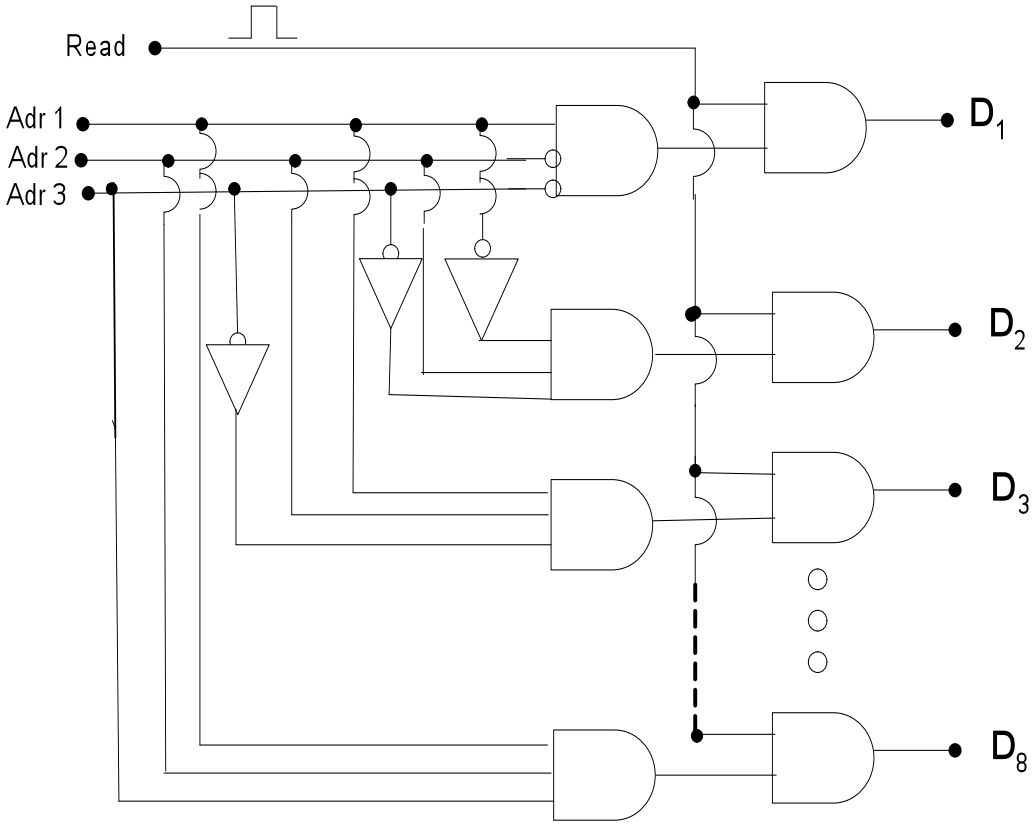


In the above example the device "looks" at address lines $A_0 - A_2$ and assert data onto data bus $D_0 - D_3$ when it sees its particular address line and it sees a READ pulse. However, there must be external logic to control 3 - state devices with the same output lines.

Data Buses (cont.)

Example of Logic Device





Data Buses (cont.)