Lecture/Laboratory #14

Lab Review

Lecture #13 Review

Multiplexers, Demultiplexers and Decoders

- Multiplexers/Select Gates
- Demultiplexers & Decoders

Programmable Array Logic (PAL)

Digital Transmission Techniques

Multiplexers, Demultiplexers and Decoders

Multiplexers/Select Gates

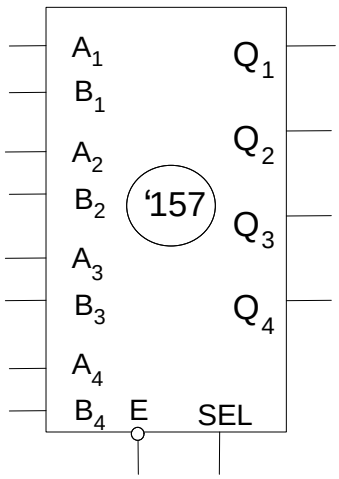
Multiplexers, which are in principle select gates, are available with 2, 4, 8, and 16 inputs.

2 – input multiplexer analysis will be based on the quad 2 – input select chip $\Rightarrow$ a 4 – pole 2 – position switch for logic signals. SELECT (SEL) = LOW $\Rightarrow Q_n = A_n$; SEL = HIGH $\Rightarrow$ $Q_n = B_n$; $\overline{ENABLE}$ ($\overline{E}$) = HIGH $\Rightarrow$ all outputs LOW (device disable).

Truth Table:

Inputs				Outputs
$\overline{E}$	SEL	A_n	B_n	Q_n
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X $\Rightarrow$ any entry



Quad Select 2 - input

‘157

Multiplexers (Select Gates) (cont.)

Chip $^{1}158$ has inverted outputs

Chip $^{1}257$ ($^{1}258$ – inverted) has 3 – state outputs.

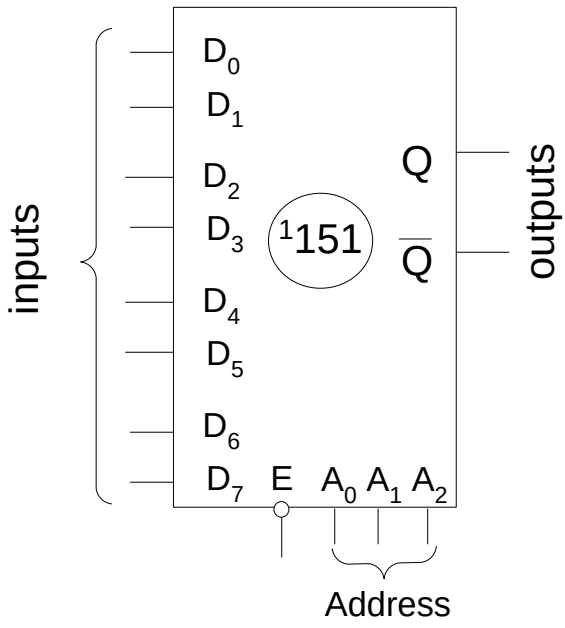
Select gates is like mechanical switch, but much better $\Rightarrow$ (a) all channels are switched simultaneously; (b) almost instantaneously switched by a logic level generated somewhere in ckt; (c) it is cheaper ; (d) less problem with generation noise.

In multiplexers $\Rightarrow$ a binary address is used to select (SELECT) input $\rightarrow$ output (which input on output)

Example: 8 – input multiplexer with 3 addresses – it address input to address the selected data input. (ENABLE is also called STROBE)

$\overline{STROBE}$ ($\overline{E}$) = *HIGH* $\Rightarrow$ $Q = LOW$

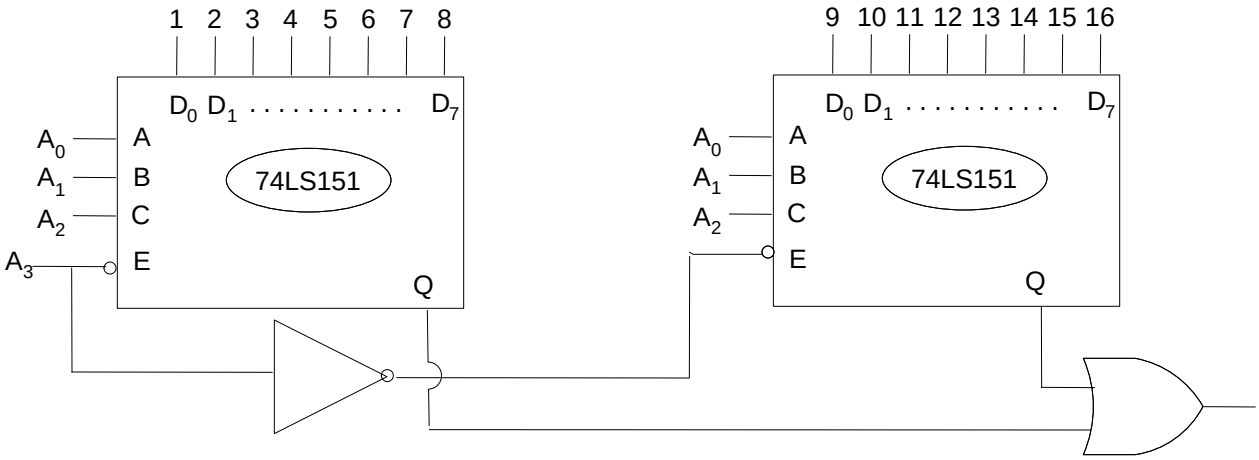
($\overline{Q}$ = HIGH) $\Rightarrow$ chip is disabled and output (LOW) is independent of inputs and address data.



Multiplexer Expansion

Multiplexer expansion (need more inputs than are provided in a given multiplexer) $\Rightarrow$ chip expansion (e.g. multiplexers, decoders, memories, arithmetic logic, etc) by using several chips that have small individual capabilities to generate a larger capability.

Example: two 8 – input 74LS151 multiplexers expended into 16 – input multiplexer.



With A_3 either chip can be enabled. Disabled chip has Q = LOW, therefore gate OR is used for final output, which depends on output of enabled chip (If outputs were 3 – state, they could be connected directly).

Demultiplexers and Decoders

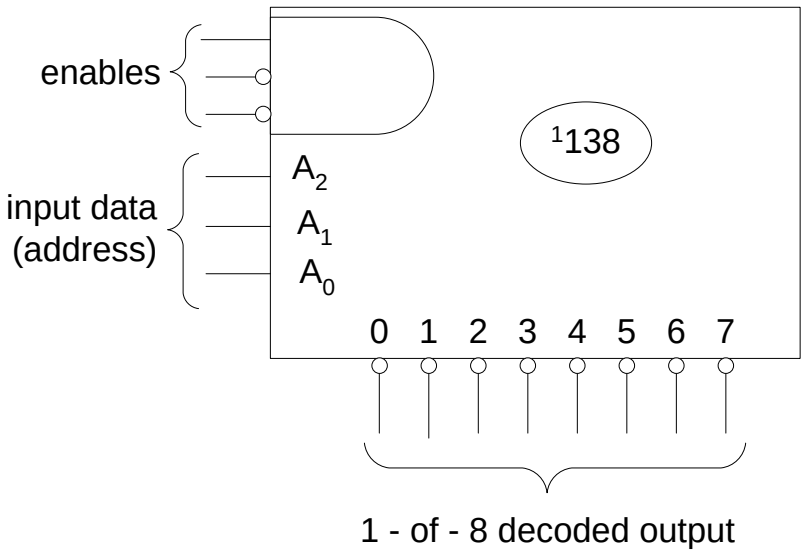
Demultiplexer connects an input to one of several possible outputs "using" instruction from address (binary address). The other outputs ⇒ in the inactive state or in open – circuit (this depends on the type of demultiplexer).

Decoder → similar, but address is only input ⇒ it is "decoded" to assert one of (n) - possible outputs.

Example: "1 – of – 8 decoder"

Output, which corresponds to addressed data is LOW, all others are HIGH.

Enables ⇒ two LOW and one HIGH, otherwise all outputs HIGH



Decoders (cont.)

Decoders are commonly used when interfacing to microprocessor, to trigger different actions depending on the address.

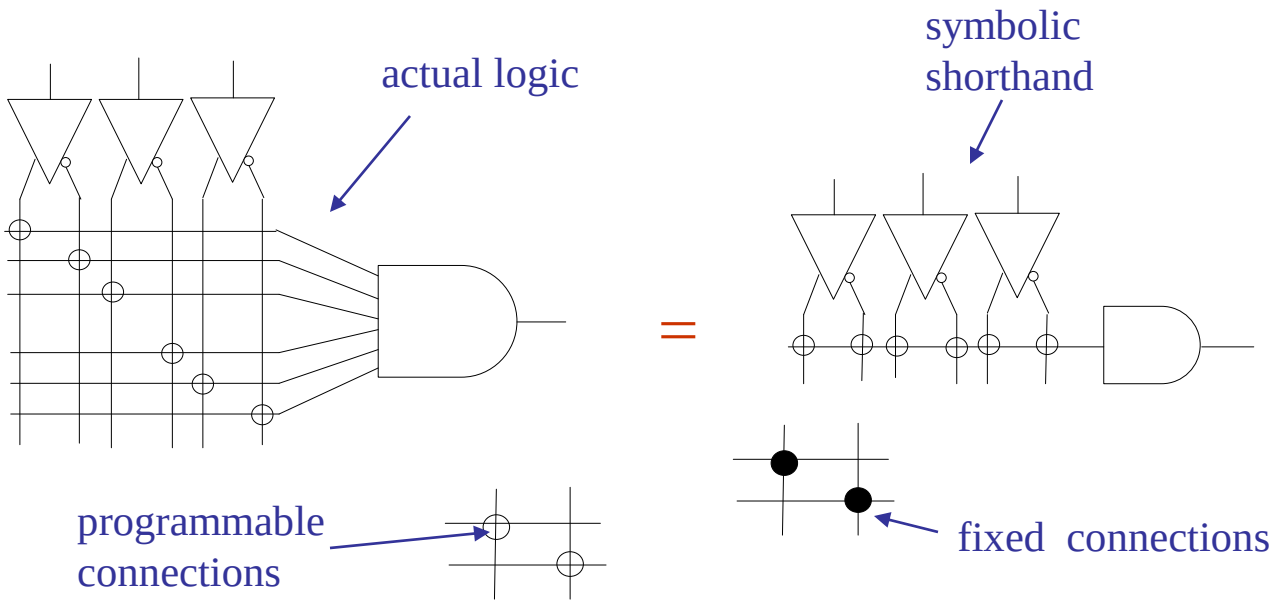
Another common use $\Rightarrow$ enable to sequence of actions in turn (directed by address from output of a binary counter).

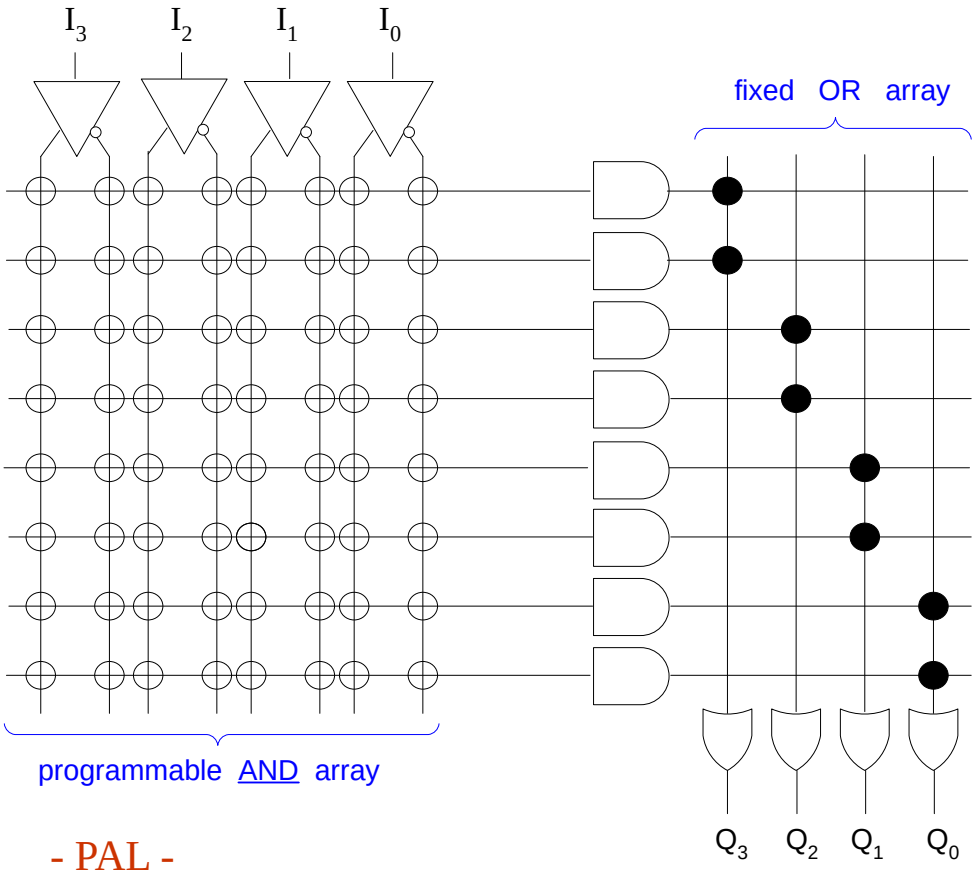
Programmable Array Logic (PAL)

PALs are ICs with many gates $\rightarrow$ interconnections can be programmed to create needed logic functions. However, limitation on interconnections by the built – in structure.

Example: PAL with programmable AND array $\Rightarrow$ for simplicity of the drawing AND and OR gates are shown with single input line; these are multiple – input gates (input corresponding to every connected crossing).

Pal (cont.)


actual logic
symbolic
shorthand
=
programmable
connections
fixed connections


I3
I2
I1
I0
fixed OR array
programmable AND array
Q3
Q2
Q1
Q0
Three - state

- PAL -

Digital Transmission Techniques

(Connections, Driving Cables, Fiber Optics)

Digital transmission techniques $\Rightarrow$ to solve the problems related to capacitive loading effects, interface pickup, transmission – line effects (impedance mismatching $\Rightarrow$ reflections) when digital signals are transmitted by cables. Knowledge of interface ICs.

- Ground current noise (spikes)
- Capacitive loads $\Rightarrow$ source of spikes
- Driving cables. Single conductor (wire) works like antenna $\Rightarrow$ pickups or generates EM (electromagnetic) signal $\Rightarrow$ creates interference between different part of electronic devices. No good!

Use $\Rightarrow$ coaxial cables, twisted pairs, flat ribbon cables (also with shielding), multiwire bundled cables fiber-optic cables.

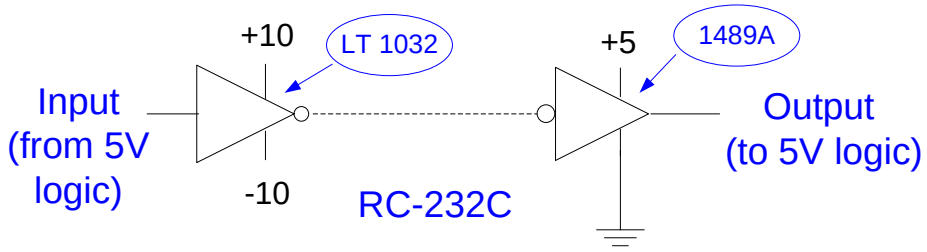
Cables or fiber-optic connections require interfacing chips to match with different parts of the system $\Rightarrow$ cables require input/output devices (drivers/receivers), fiber-optics need also couplers, which change electrical signal to optical signal (driver), and at the end of line change optical to electrical signal.

Digital Transmission Techniques (cont.)

Digital interfacing ⇒ RS-232

RS-232 C (or RS-232 D) is interface chip for relatively slow transmission (~ 1 k bits/sec) through simple multiwire cables. RS-232 is relatively insensitive to noise.

Scheme:

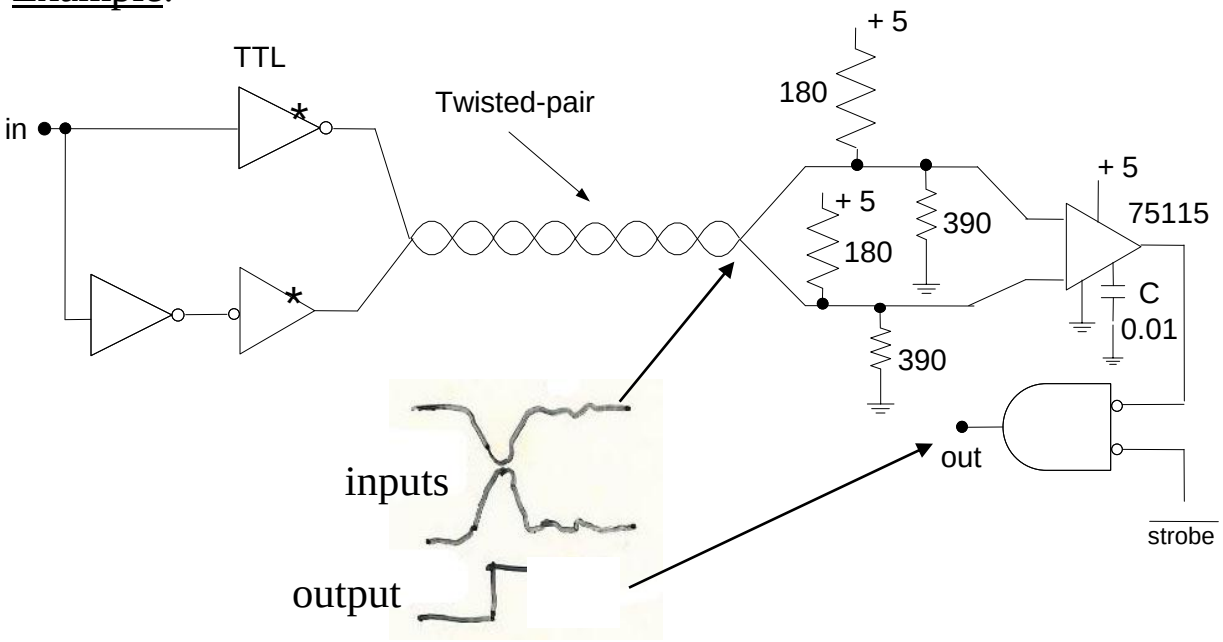


RC-232 is being used extensively for communication between computers and terminals. Max rates ~ 38 kbits/sec.

Differential Drive: RS -422

Using twisted-pair cable and differential signal receiver, one can obtain much better noise immunity and higher transmission rate:

Example:



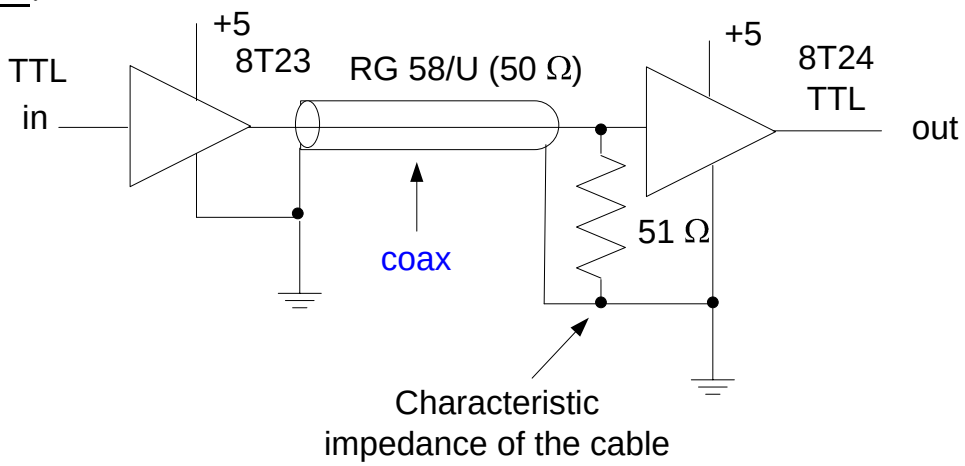
Paired TTL inverters drive a twisted-pair with true and complemented signals. Differential receiver 75115 regenerate clean TTL levels, rejecting noise. TTL are used (instead of CMOS) for their better resistance to static electricity damage. This system has low reflection of the signal at the end of transmission line because good match to receiver impedance.

Coaxial – Cable Drivers

Coaxial cable → excellent protection against interference (completely shielded geometry)

→ predictable impedance (uniformity of diameter and spacing).

Example 1:



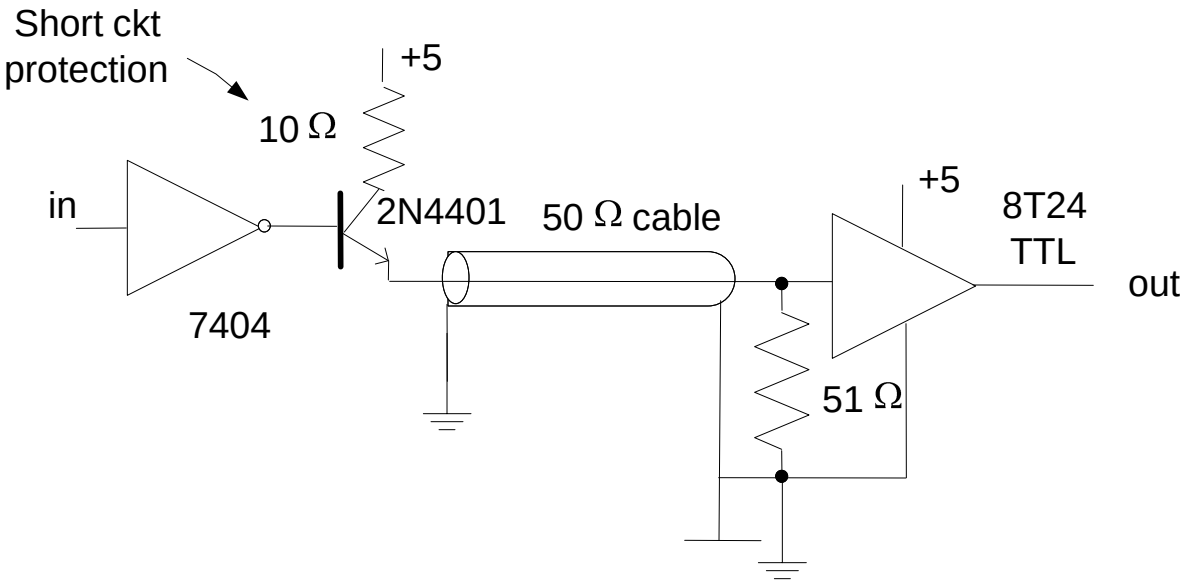
8T23 drivers 50 Ω load.

Max bit rates for 1 mile cable = ~ 100 kb/sec

short cable ⇒ ~ 20 Mb/sec

Coaxial – Cable Drivers (cont.)

Example 2: Driver: Emitter follower 2N4401



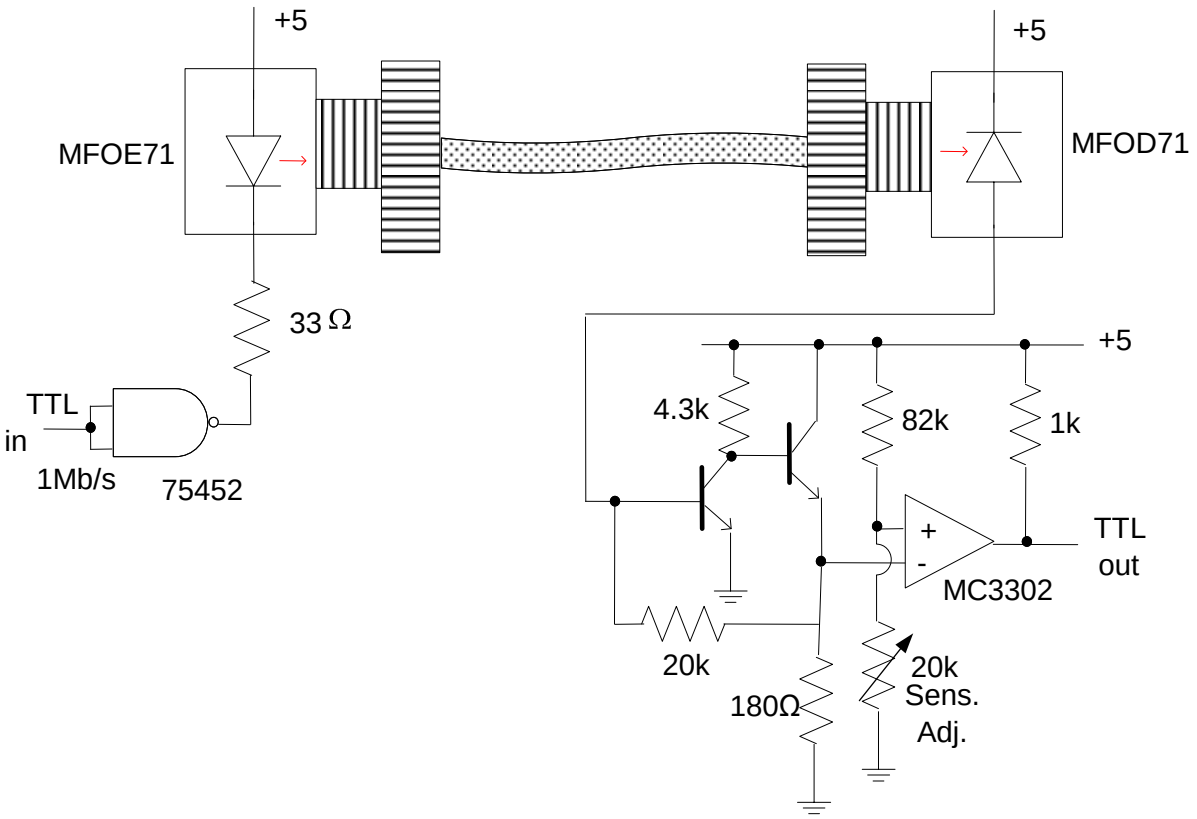
Fiber – Optic Cables

F – O cables: - no EM noise effect

- very large bandwidths (several GHz)
- very low losses at large distances
- negligible dispersion

Fiber – Optic Cables (cont.)

Example:



Inexpensive set of driver/receiver by Motorola (MFOE71/OD71)

Data rate: up to 1 Mb/sec (for 30 feet fiber) → plastic

Higher performance: glass and quartz fibers.

Best performance: 4 GHz for 120 km without repeaters (very fast progress)