Lecture/laboratory #15/16

Review of Lab

Review of Lecture #14

Bit – serial transmission

ASC II code

Introduction to UART and USART

Introduction to memory

- RAM, ROM

Static RAM (S – RAM) and Dynamic RAM (D – RAM)

Discussion of S – RAM for DSO use

Bit – Serial Transmission

Any alphanumeric code (e.g. ASCII, which will be described later) can be transmitted either as a parallel 8 – bit group (8 separate wires) or as a serial string of 8 bits one after the other (1 wire).

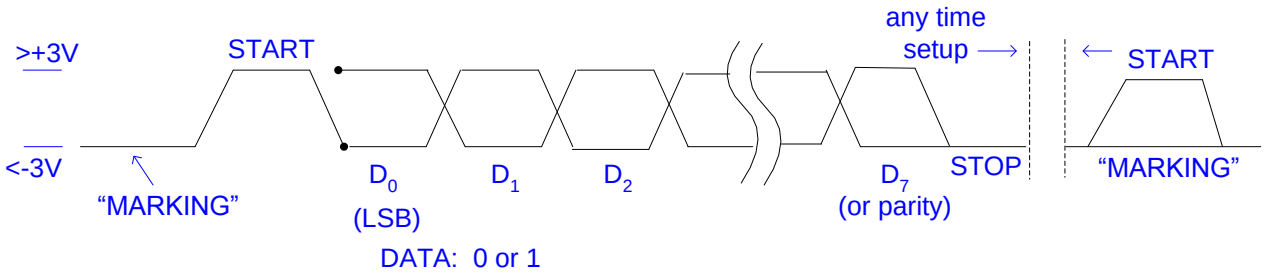
Such serial transmission it is convenient to use when we deal with relatively low or moderately fast transmission speed.

Serial transmission has a standard bit – transmission protocol and a fixed bit rates: for asynchronous transmission, a (asynchronous vs. synchronous processes → below) start bit and a stop bit (sometimes two) are attached to the ends of each 8 – bit character, forming 10 – bit group.

The sender and receiver use a fixed bit rate ⇒ popular but rates: 300, 1200 2400, 4800, 9600, and 19,200 band (bit/sec)

Bit – Serial Transmission (cont.)

Timing waveform for serial transmission:



When no information is being sent → transmitter is in "MARKING" state.

Every character begins with a START bit, followed by the 8 ASC II bits with LSB being first (usually 7 data bits and 1 optional parity bit), and a final STOP bit (STOP bit has to be at least one clock period, but may extend any amount longer.

At the receiving end ⇒ UART (Universal asynchronous receiver (transmitter), which is operating at the same band rate synchronizes to each 10 – bit group, generating successive 8 – bit parallel data groups from the input serial string.

Because START and STOP bits, which determined beginning and the end of each character, the receiver doesn't require highly accurate clock ⇒ transmitter and receiver have to be synchronized to a fraction of bit period over the time of one character (i.e. ~ a few percent accuracy).

Bit – Serial Transmission (cont.)

The UART is triggered at the beginning of the START bit, waits for ½ bit to check if START is still on, and then examines the data value at the middle of each data cell. The STOP bit terminates the character → resting state until a new characters are sent.

The UART looks for STOP bit 10.5 bit – intervals after START to help verify a correctly sent character. Modern UART has programmable band – rate generators.

American Standard Code for Information Interchange ASCII, is 7 – bit code. However, in bit – serial transmission with ASC II practically always 8^{th} bit is transmitting, although it is not part of ASCII. This 8^{th} bit is used for parity (odd or even) indication or is occasionally used as a shift key to generate an additional 128 characters. (e.g. Greek symbols). This 8^{th} bit may be sued for transmission binary data via serial connections.

ASII consists of non-printing and printing characters; non – printing → control characters. The are used to control printing or program execution.

Table for ASC II Code

Name	Control char	non-printing Char	Hex	Dec	printing Char	Hex	Dec	printing Char	Hex	Dec	printing Char	Hex	Dec
null	ctrl-@	NUL	00	00	SP	20	32	@	40	64	`	60	96
start of heading	ctrl-A	SOH	01	01	!	21	33	A	41	65	a	61	97
start of text	ctrl-B	STX	02	02	"	22	34	B	42	66	b	62	98
end of text	ctrl-C	ETX	03	03	#	23	35	C	43	67	c	63	99
end of xmit	ctrl-D	EOT	04	04	$	24	36	D	44	68	d	64	100
enquiry	ctrl-E	ENQ	05	05	%	25	37	E	45	69	e	65	101
acknowledge	ctrl-F	ACK	06	06	&	26	38	F	46	70	f	66	102
bell	ctrl-G	BEL	07	07	'	27	39	G	47	71	g	67	103
backspace	ctrl-H	BS	08	08	(	28	40	H	48	72	h	68	104
horizontal tab	ctrl-I	HT	09	09	)	29	41	I	49	73	i	69	105
line feed	ctrl-J	LF	0A	10	*	2A	42	J	4A	74	j	6A	106
vertical tab	ctrl-K	VT	0B	11	+	2B	43	K	4B	75	k	6B	107
form feed	ctrl-L	FF	0C	12	,	2C	44	L	4C	76	l	6C	108
carriage return	ctrl-M	CR	0D	13	-	2D	45	M	4D	77	m	6D	109
shift out	ctrl-N	SO	0E	14	.	2E	46	N	4E	78	n	6E	110
shift in	ctrl-O	SI	0F	15	/	2F	47	O	4F	79	o	6F	111
data line escape	ctrl-P	DLE	10	16	0	30	48	P	50	80	p	70	112
device control 1	ctrl-Q	DC1	11	17	1	31	49	Q	51	81	q	71	113
device control 2	ctrl-R	DC2	12	18	2	32	50	R	52	82	r	72	114
device control 3	ctrl-S	DC3	13	19	3	33	51	S	53	83	s	73	115
device control 4	ctrl-T	DC4	14	20	4	34	52	T	54	84	t	74	116
neg acknowledge	ctrl-U	NAK	15	21	5	35	53	U	55	85	u	75	117
synchronous idle	ctrl-V	SYN	16	22	6	36	54	V	56	86	v	76	118
end of xmit block	ctrl-W	ETB	17	23	7	37	55	W	57	87	w	77	119
cancel	ctrl-X	CAN	18	24	8	38	56	X	58	88	x	78	120
end of medium	ctrl-Y	EM	19	25	9	39	57	Y	59	89	y	79	121
substitute	ctrl-Z	SUB	1A	26	:	3A	58	Z	5A	90	z	7A	122
escape	ctrl-[	ESC	1B	27	;	3B	59	[	5B	91	{	7B	123
file separator	ctrl-\	FS	1C	28	<	3C	60	\	5C	92	|	7C	124
group separator	ctrl-]	GS	1D	29	=	3D	61	]	5D	93	}	7D	125
record separator	ctrl-^	RS	1E	30	>	3E	62	^	5E	94	~	7E	126
unit separator	ctrl-_	US	1F	31	?	3F	63	_	5F	95	DEL	7F	127

E.g. key CRTL + Letter $\Rightarrow$ any (chosen) control

CTRL + M $\Rightarrow$ CR

NUL (null) $\Rightarrow$ all zeros (to delimit character strings)

DC3 $\Rightarrow$ "soft handshake" (to stop transmission)

Synchronous vs. Asynchronous Communication

Synchronous exchange of data $\Rightarrow$ data is asserted onto or retrieved from the bus synchronously with strobing signals (clock)

Asynchronous transmission of data $\Rightarrow$ data IN: ADDRESS on device and IN on control line. This correlates data IN with addressed device. The addressed device asserts the DATA and level "informing" that DATA is valid ("DATA READY").

When control device (e.g. CPU in computer) "sees" DATA READY, it latches the DATA and then releases its IN level for transmission of the data.

Synchronously transferring systems are much simpler than asynchronously transferring systems.

However, asynchronous transmissions are more reliable, no limitations on length of DATA (nevertheless in modern computers synchronous transmission is used)

UART and USART

Universal Asynchronous Receiver/Transmitter (UART) or Univ. Synchronous/Asynchronous Receiver/Transmitter (USART) are chips (microprocessor – controlled) which convert parallel data (usually 8 – bit words) to a serial data stream for transmission over single – wire cable and simultaneously convert received serial bit stream to parallel words.

UARTs and USARTs are most often used to send data to and from terminals, nard-copy devices, modems or directly between computers. Usual method of operation: to use serial-transmission of ASC II via RS-232. In such simple form of communication UART is used or USART is used in asynchronous mode.

Each 8 – bit character is headed by START bit and ended by STOP bit $\Rightarrow$ together transmitted as 10 – bit serial string at a standard band rate.

Some chips being used: UART 8250 (Nat.) (in IBM PC); USART 8251 (from Intel Co.) USART 8530 (popular, used in Macintosh).

UART and USART (cont.)

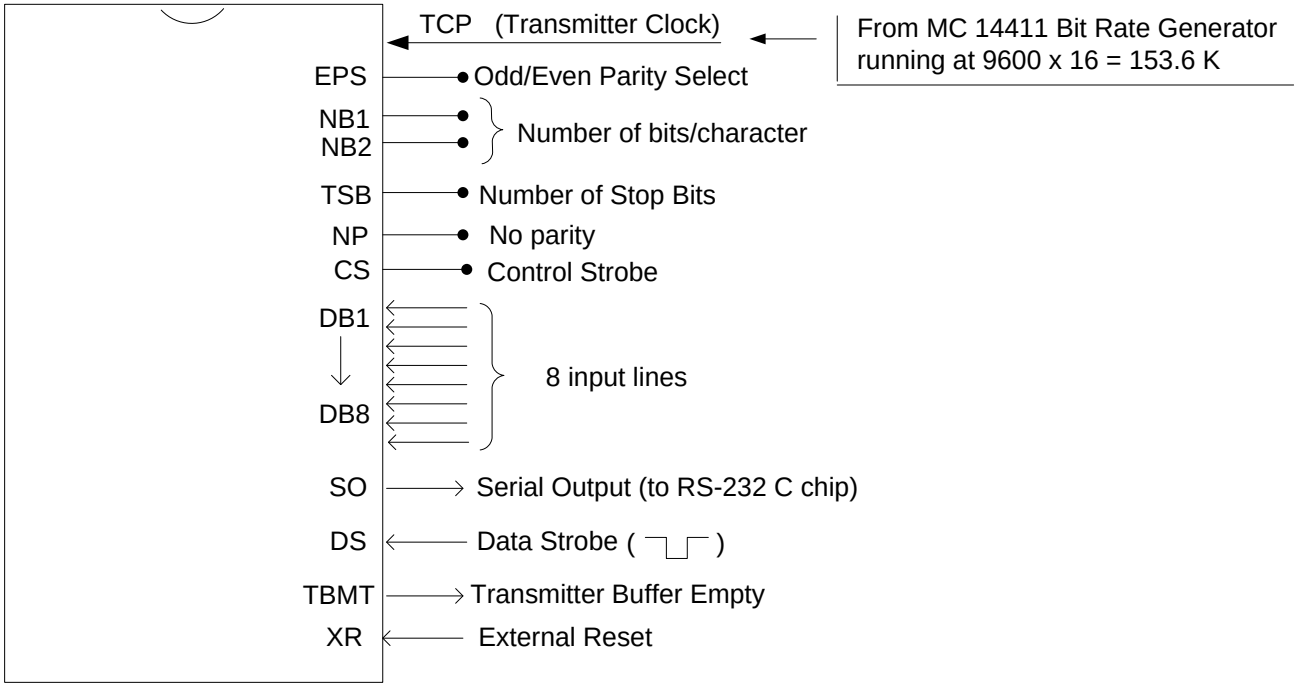
USARTs usually include a programmable band-rate generator, flexible control of bit format (number of bits, parity, etc.). The most advanced USARTs also have different modulation methods, powerful synchronous modes of operation, error checking, clock recovery, block data transfer to control devices etc.

For DSO you will be using UART AY-3-1015D, which is much simpler for operation (but also much less felxible) than the USART 8530.

The AY-3-1015D will be used to send the digitized signal from Random Access Memory (RAM) to the IBM PC over Rs-232 line. The UAER chip is complimented by two other chips: a bit rate generator and RS-232 line signal adjuster.

UART and USART (cont.)

Example: UART AY-3-1015D in transmission mode



The function of each pin can be found in the Technical DATA of AY-3-1015D. Some of these functions are presented here for UART in transmission mode:

Transmitter clock (TCP) line is connected with clock (bit rate generator), which has to have frequency 16 – times higher than transmitter rate.

UART (cont.)

EPS: "1" for even parity, "0" for odd parity

NB1, NB2 (Number of bits/character): For selection 5, 6, 7 or 8 data bits/character (e.g. 0, 0 ⇒ 5; 1, 0 ⇒ 6; 0, 1 ⇒ 7; 1, 1 ⇒ 8)

Number of Stop Bits (TSB): Selection of 1 or 2 STOPs at the end of Data (after parity) ⇒ logic "0" for 1 STOP, and "1" for 2 STOPs.

No Parity (NP): "1" → eliminate the parity bit; a "stop" bit will immediately follow last data bit.

Control Strobe (CS): "1" will allow to enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding.

DB1 – DB8: 8 data bit input lines

Serial output (SO): serial transmission of characters (bit – by – bit). "1" – for no transmission.

Data Strobe (DS): Rising edge of DS will initiate data transmission into data bits holding register.

Transmitter buffer Empty (TBMI): goes to "1" when the data bits holding register is available (ready) to be loaded with another character.

External Reset (XR): Provides reset for all registers except the control register (⇒ "1")

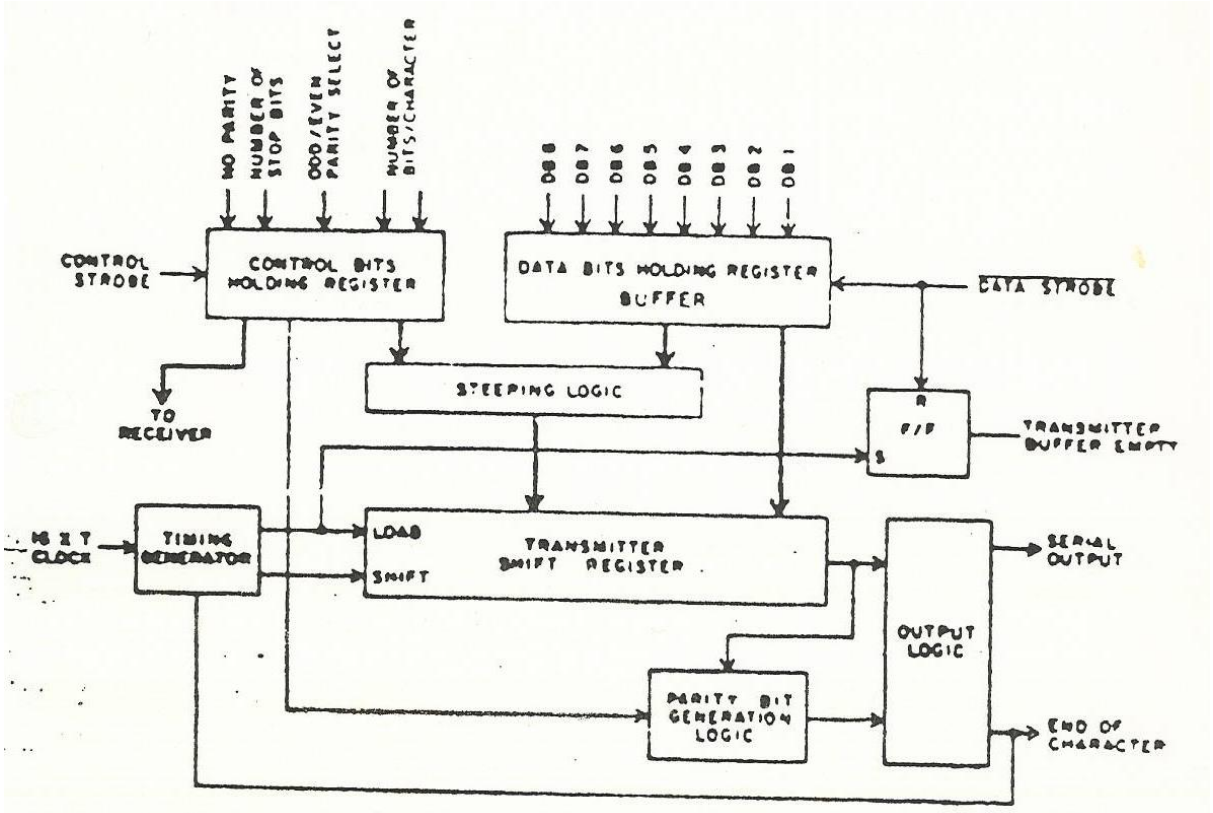


Fig. 2 TRANSMITTER BLOCK DIAGRAM

BLOCK DIAGRAM

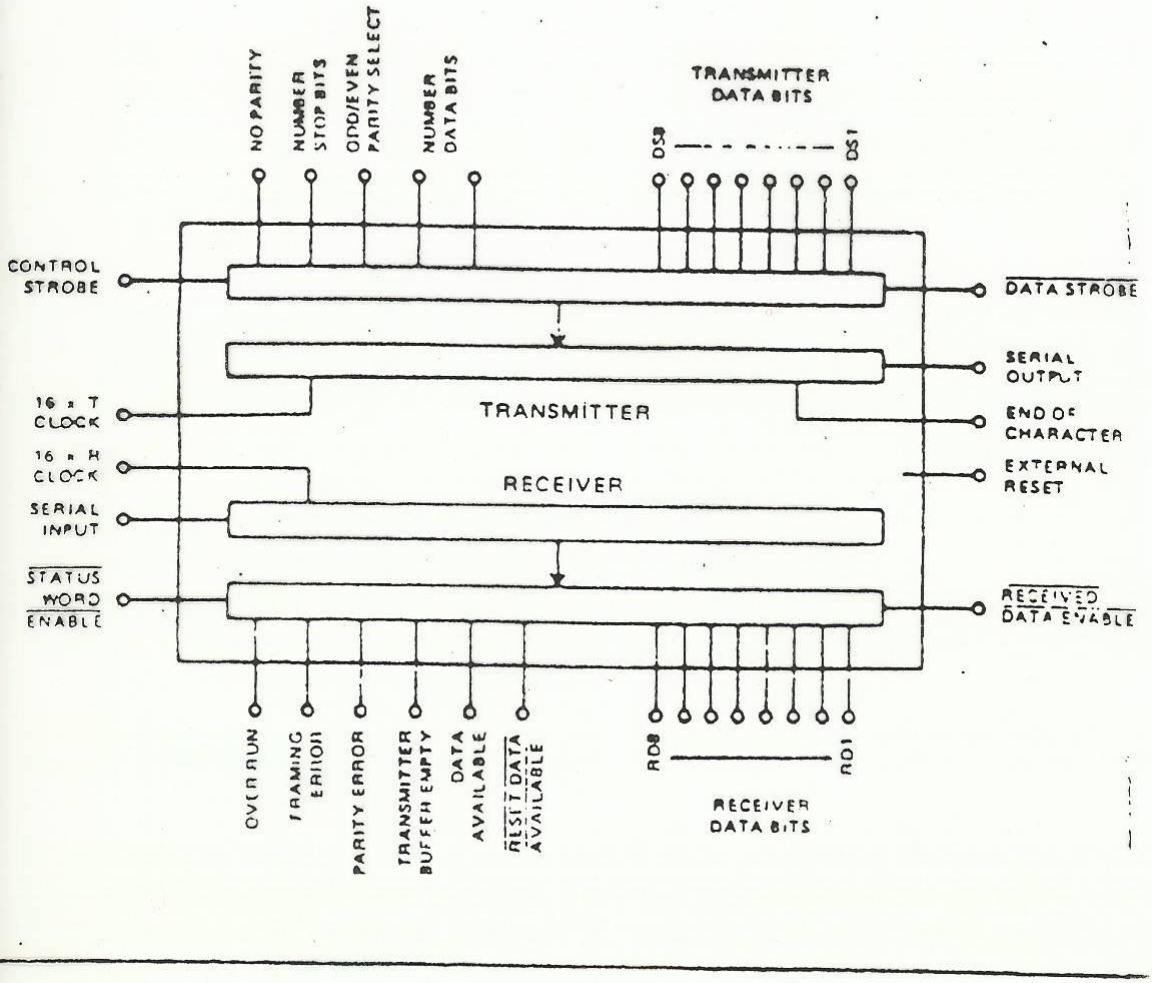


Figure 1

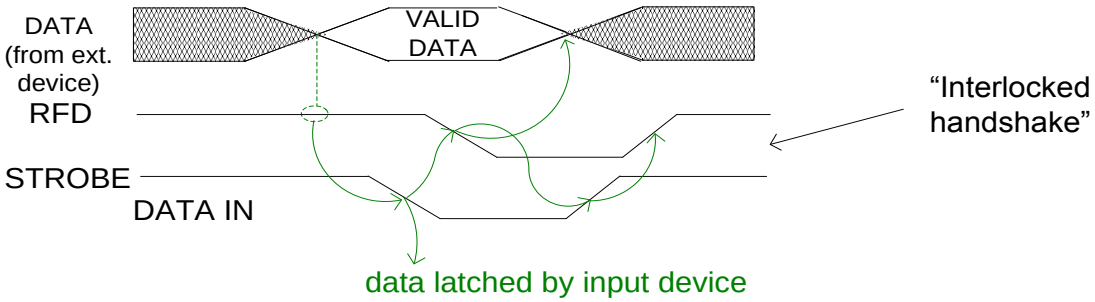
Operation of UART (cont.)

With “power – on”, XR → enabled, clock pulse → on (16 x higher than desired band) the TBMT and SO will to “1”, and DS pulsed make TBMT goes “0” until previous character (“old” one) will be transmitted, which again will be signaled by TBMT goes “1”. For UART “working” with computer, on command from computer the RAM is read and data sent through UART to the computer (e.g. IBM PC). Computer provides “friendly” interactions (“handshaking”), which is described below.

“Handshaking”

“Handshaking” is the communication process between e.g. external device and processor. Let’s assume that external device is sending data to the processor and it “wants to know” when input device is ready to accept the next byte of the data. “Ready for data”, RFD, output from input/output device provides solution. I/O device open the line when byte has been transmitted to computer (processor).

Example of analysis:



"Handshaking" (cont.)

"Interlocked handshaking" ⇒ data IN: the external device (source) could assert data, but waits for RFD before asserting the STROBE. It releases the STROBE when it sees RFD disasserted, then waits for RFD again.

The handshake is fully interlocked ⇒ each side in the transaction waits for the other to complete each step. This fully interlocked data exchange guarantees that no data is lost.

Memory: RAM and ROM

RAM: Random Access Memory ⇒ large variety in size
(~ 10K → G bytes); K = 1024 = 2^{10} ; k = 1000.
RAM is fast: 100 ns for read - out or write – out.

RAM is volatile: ⇒ information evaporates when power is off.

Non volatile memory is ROM (Read – Only – Memory), which is necessary to start computer when power is first turned on. Additional ROM is often used for system routines, graphics routines and other programs that are required (desired) to be on all the time.

Memory: RAM and ROM (cont.)

To get or store information in memory, the Central Processing Unite (CPU) addresses the desired word. Most computers address memory by bytes, beginning at byte 0 and going sequentially through to the last byte in memory.

Because most computer words are several bytes long, the computer is storing or retracting from memory a group of bytes rather than separate bytes a time.

In computer with lots of memory, it takes three or four bytes to specify and address in memory.

RAM: static RAM (S – RAM) and dynamic RAM (D – RAM).

S – RAM stores bits in array of flip – flops

D – RAM stores bits as charged capacitors.

In S – RAM a bit written in stays there until rewritten or until power is off.

In D – RAM data will disappear in ~ 1 sec unless "refreshed" → periodic clocking through the two-dimensional pattern of bits in the chip. E.g. in 256 K-bit RAM each of 256 row addresses have to be accessed every 4 ms. D-RAM is more compact than S-RAM and less expensive. However, S-RAM is more simple → no need for refreshing clocks, it avoids timing complexity ⇒ for small systems S-RAM is the best choice.

Memory (cont.)

Most S – RAM is CMOS → low energy consumption (important for battery use). S – RAM (CMOS) with battery backed up (when main power is off) forms alt. to ROM. S – RAM is available in high-speed version (≤ 25 ns).

Popular S – RAM 6116 (2K x 8 – bit) and 6264 (8K x 8 – bit). The 6264 is more recent one. Both are available in the Lab.

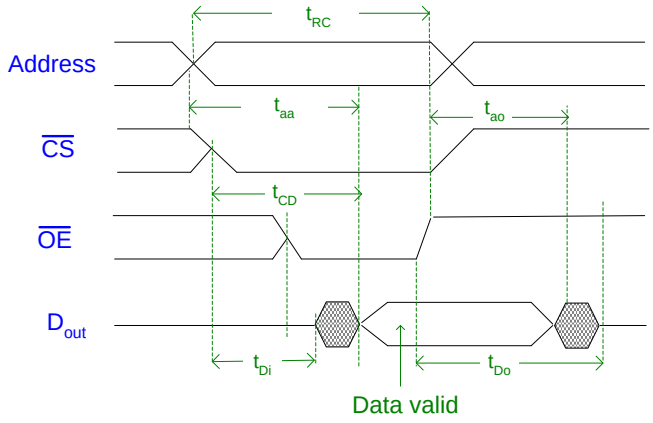
Analysis of S – RAM (timing waveform) for READ:

Read Cycle Time t_{RC} ↓

$t_{RC} \approx >$ 100 – 150 nsec dependent on model)

$t_{aa} \approx \leq t_{RC}$; $t_{ao} \approx \geq$ 10 nsec

$t_{Di} \geq$ 10 nsec ; $t_{Do} \leq$ 40 nsec

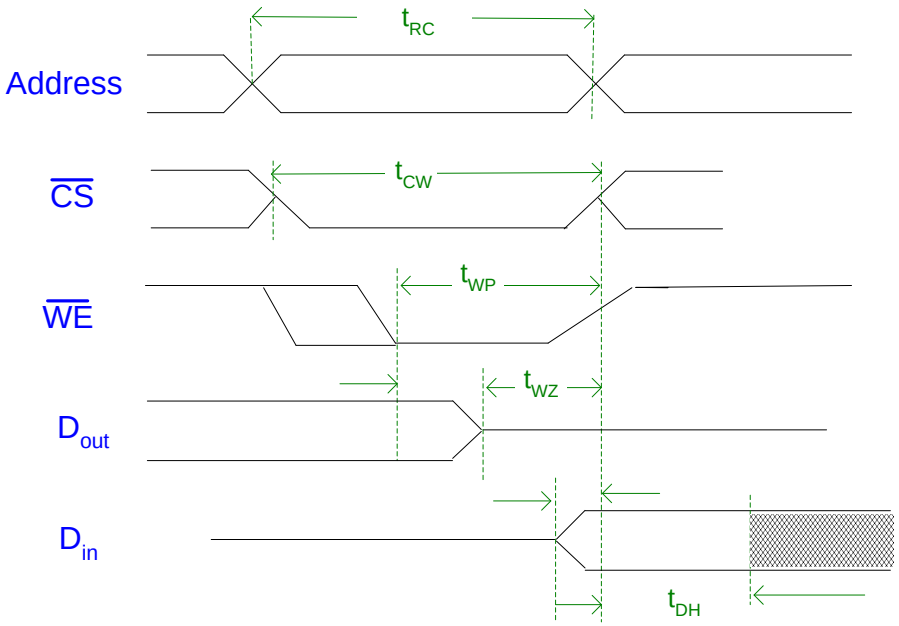


Assert address and then Chip Select $(\overline{CS})$ and Output Enable $(\overline{OE})$ for READ. The requested data appears on the three – state data lines after $t_{aa} \approx$ 100 – 150 nsec (or less) → address access time. Speed for the memory : the time from assertion of valid address to valid data (read).

Memory (cont.)

Analysis of S – RAM for WRITE:

First : assert address + data and $(\overline{CS})$. Then (after and address setup time t_{as}) : Write Enable $(\overline{WE}) \Rightarrow$ valid data are written at the end of $(\overline{WE})$ pulse.



t_{WC} - write cycle time $\geq 100 – 150$ ns

t_{CW} – chip selection time to end of write (end of $\overline{WE}$ pulse)

t_{WP} – pulse width for WRITE

t_{WZ} – write to output

t_{DH} – data hold

Dynamic RAM (D – RAM)

D – RAM is more complicated for analysis than S – RAM. (In general D – RAM is more complex). One of the major problems with D-RAM is to maintain all strobes and address lines noise-free $\Rightarrow$ address lines and other control signals connected (bused) to a few dozen of chips over significant area of PC board $\Rightarrow$ needs significant current, fast switching $\Rightarrow$ generates noise.

ROM (Read Only Memory) – nonvolatile $\Rightarrow$ several choices:

(a) EPROM – UV – erasable

(b) EEPROM – electrically erasable

(c) Mask-programmed and fusible – link ROM

EPROM: Large chip with quartz window, popular; available in CMOS and NMOS. Connections between gates can be programmed by breakdown of their insulating layers with $V > 20$ volts. Storage data: by retaining indefinitely a small charge ($\sim 10^6$ electrons) on these insulated gates (working like capacitors with indefinitely long time constant). Each of such "capacitor" state can be read out as being the gate of an associated MOSFET channel. Since the gates are not electrically accessible they can be erased only for exposing them to intense UV radiation for 10 – 30 min. This causes the stored charge to leak off by photoconduction $\Rightarrow$ no selective erase possible.

Memory → ROM (cont.)

EPROMs range: 8K x 8 → 128K x 8 typically access time (typical) = 150 – 300 ns, although can be as fast as 25 ns.

EPROMs are very good for prototype development (they can be re-used after they're erased).

Data retention: > 10 years!

Erase/program cycles ≈ 100 (= limited endurance)

EPROM pins can match RAM pins, so it is easy to exchange.

In Lab → EPROM with quartz window

EEPROM ⇒ selectively erased and reprogrammed electrically, while in-circuit.

EEPROMs: ideal for holding configuration information, calibration parameters and so on, that cannot be frozen before the computer or instrument is used.

They used the same MOSFET floating – gate technique as EPROMs.

Recently available EEPROMs run from a single +5V power supply and work nearly the same as S-RAMs ⇒ any byte can be reprogrammed with a single bus WRITE cycle.

These EEPROMs use internal circuitry to generate higher programming voltages.

Memory → ROM (cont.)

Internal logic latches the data and generates several – millisecond programming sequence. They can be connected to the circuit the same way as S – RAMs ⇒ the same socket as S – RAMS and the same circuit ⇒ BUSY line in such case is used for READ data to EEPROM. It is necessary to include in program the read-back data procedure, which also requires waiting to check for agreement with data written.

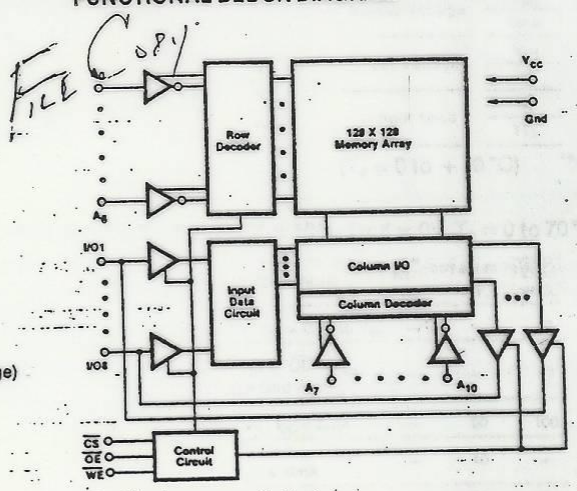
CMOS EEPROMs are available in 2K x 8 → 32k x 8 range (~ $10 - $50); access time ~ 200 – 300 nsec; programming speeds: ~ 2 ms/byte ; they are great for prototypes.

CMOS STATIC RAMS 16K (2K X 8 BIT) 6116S 6116L

Device Technology Inc.

- ...eed (equal access and cycle time)
- ...T 6116S-70/90/120: 70ns/90ns/120ns (max.)
- ...T 6116L-90/120/150: 90ns/120ns/150ns (max.)
- ...power consumption
- ...T 6116S
  - Active: 180mw (Typ.)
  - Standby: 100μw (Typ.)
- ...T 6116L
  - Active: 160mw (Typ.)
  - Standby: 20μw (Typ.)
- ...gle 5V (±10%) power supply
- ...t and output directly TTL compatible
- ...ree state output
- ...ndard 24 pin dual-In-line plastic package
- ...e compatible with standard 16K Static RAM ...d EPROM
- ...ttery back up operation (2V data retention voltage) ...T 6116 L only)

FUNCTIONAL BLOCK DIAGRAM



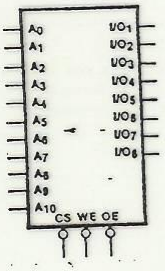
...UTH TABLE

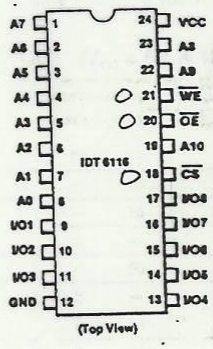
...	CS	OE	WE	I/O OPERATION
...	H	X	X	High Z
...	L	L	H	D_{out}
...	L	H	H	High Z
...	L	X	L	D_{in}

PIN CONFIGURATION

A_0-A_{10}: Address
I/O1-I/O8: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{cc}, Gnd

...GIC SYMBOL





October 1981

INTEGRATED DEVICE TECHNOLOGY, INC.
3236 Scott Blvd., Santa Clara, CA 95051 • Telephone: (408) 727-6116 • TWX 9103382070

PRELIMINARY

2K × 8 CMOS STATIC RAM
MK6116 (J/N) - 15/20/25
MK6116L (J/N) - 15/20/25

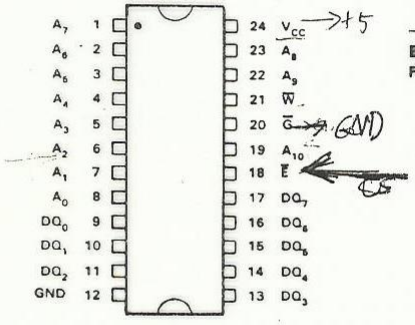
FEATURES

- ☐ Direct replacement for 2K × 8 Byte Wide Static RAM
- ☐ +5 Volt only Read/Write
- ☐ 24-Pin Dual in Line package, JEDEC pinout
- ☐ Read Cycle time equals write cycle time
- ☐ High Performance

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0 - DQ_7	Data In/Data Out		

PIN CONNECTIONS
Figure 1



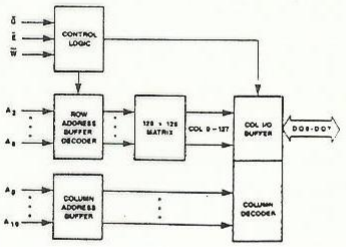
TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
V_{IH}	X	X	Deselect	High Z	Standby
V_{IL}	X	V_{IL}	Write	D_{IN}	Active
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active

Part No.	Access Time	R/W Cycle Time
MK6116/L-25	250 nsec	250 nsec
MK6116/L-20	200 nsec	200 nsec
MK6116/L-15	150 nsec	150 nsec

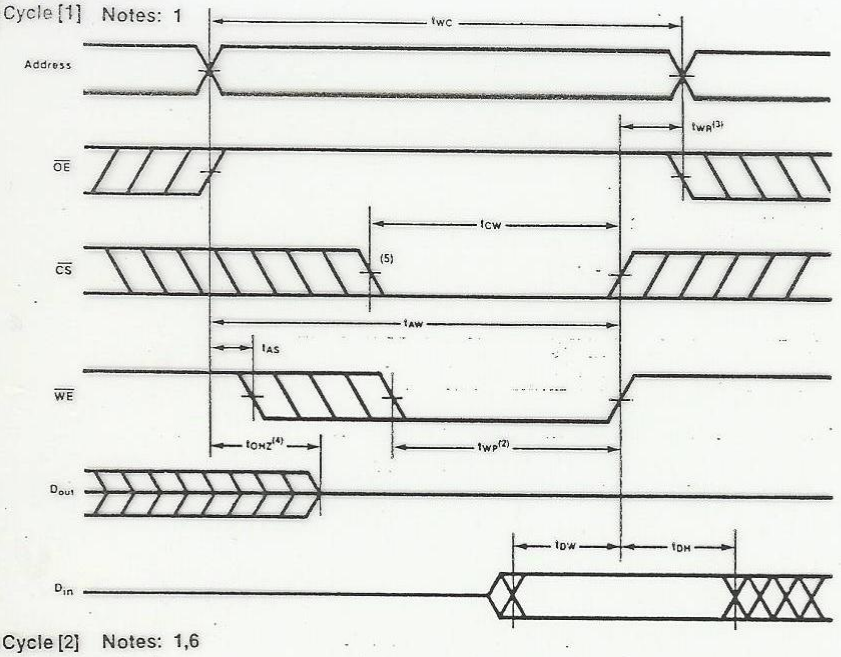
DESCRIPTION
The MK6116/6116L are 16,384-bit, CMOS Static RAMS, organized 2K × 8 using advanced HCMOS process technology. They are direct replacements for the popular 24-pin 6116/6116L type static CMOS RAMS. Both devices have the same functional operating characteristics except for active and standby power levels.

BLOCK DIAGRAM
Figure 2

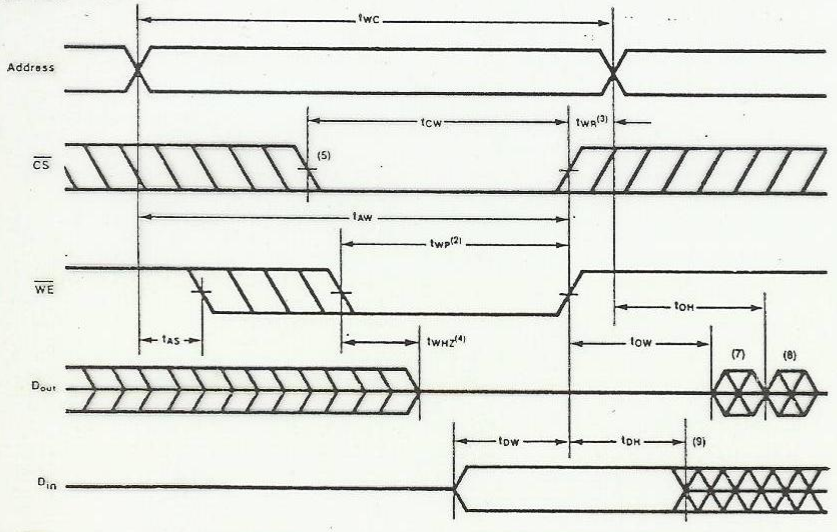


ING WAVEFORMS

Write Cycle [1] Notes: 1



Write Cycle [2] Notes: 1,6



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continously low. ($\overline{OE} = V_{IL}$.)
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

Integrated Device Technology

MEMORY

Integrated Device Technology, Inc.

6116S AC CHARACTERISTICS-WRITE CYCLE (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

ITEM	SYMBOL	IDT6116S-70 MIN.	IDT6116S-70 MAX.	IDT6116S-90 MIN.	IDT6116S-90 MAX.	IDT6116S-120 MIN.	IDT6116S-120 MAX.	UNIT
e Time	t_{WC}	70	—	90	—	120	—	ns
Selection to End of Write	t_{CW}	40	—	55	—	70	—	ns
ess Valid to End of Write	t_{AW}	65	—	80	—	105	—	ns
ess Set-up Time	t_{AS}	15	—	15	—	20	—	ns
e Pulse Width	t_{WP}	40	—	55	—	70	—	ns
e Recovery Time	t_{WR}	5	—	5	—	5	—	ns
ut Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	40	ns
e to Output in High Z	t_{WHZ}	0	40	0	50	0	50	ns
a to Write Time Overlap	t_{DW}	30	—	30	—	35	—	ns
a Hold from Write Time	t_{DH}	5	—	5	—	5	—	ns
ut Active from End of Write	t_{OW}	0	—	0	—	5	—	ns

6116L DC CHARACTERISTICS (V_{CC} = 5V ± 10%, Gnd = 0V, T_a = 0 to 70°C)

ITEM	SYMBOL	TEST CONDITIONS	IDT6116L-90 MIN.	IDT6116L-90 TYP.	IDT6116L-90 MAX.	IDT6116L-120/150 MIN.	IDT6116L-120/150 TYP.	IDT6116L-120/150 MAX.	UNIT
t Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = Gnd to V_{CC}	—	—	2	—	—	2	µA
ut Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = Gnd to V_{CC}	—	—	2	—	—	2	µA
rating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	80	—	35/30	70/60	mA
	I_{CC1}	V_{IH} = 3.5V, V_{IL} = .6V, $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
rage Operating Current	I_{CC2}	Min. Cycle, duty = 100%	—	40	80	—	35/30	70/60	mA
ower Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	5	15	—	4	12	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}$ − .2V, $V_{IN} \geq V_{CC}$ − .2V or $V_{IN} \leq$ .2V	—	4	100	—	4	100	µA
utput Voltage	V_{OL}	**I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

= 5V, T_a = 25°C

**I_{OL} = 2.1mA for IDT6116LP-150

TEST CONDITIONS

nput pulse levels: 0.8V to 2.4V
nput rise and fall times: 10ns
Input and output timing reference levels: 1.5V
Output load: 1TTL gate and C_L = 100 pF (including scope and jig)

6116L AC CHARACTERISTICS-READ CYCLE (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

ITEM	SYMBOL	IDT6116L-90 MIN.	IDT6116L-90 MAX.	IDT6116L-120 MIN.	IDT6116L-120 MAX.	IDT6116L-150 MIN.	IDT6116L-150 MAX.	UNIT
d Cycle Time	t_{RC}	90	—	120	—	150	—	ns
ess Access Time	t_{AA}	—	90	—	120	—	150	ns
Select Access Time	t_{ACS}	—	90	—	120	—	150	ns
Selection to Output in Low Z	t_{CLZ}	5	—	10	—	15	—	ns
ut Enable to Output Valid	t_{OE}	—	65	—	80	—	100	ns
ut Enable to Output in Low Z	t_{OLZ}	5	—	10	—	15	—	ns
Selection to Output in High Z	t_{CHZ}	0	40	0	40	0	50	ns
ut Disable to Output in High Z	t_{OHZ}	0	40	0	40	0	50	ns
ut Hold from Address Change	t_{OH}	5	—	10	—	15	—	ns

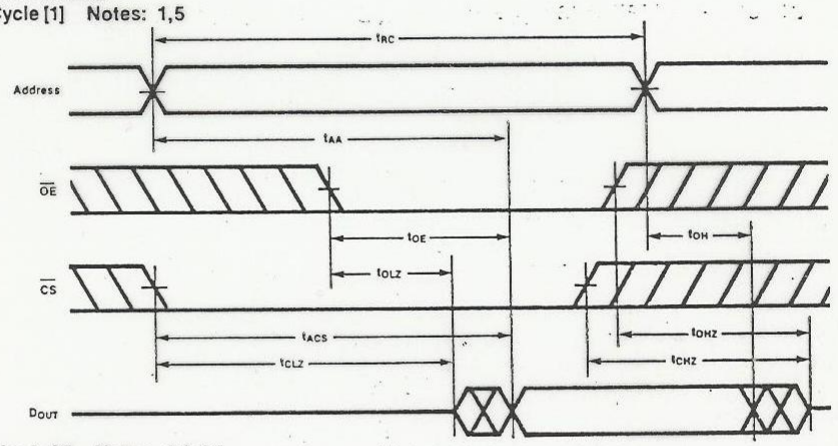
Integrated Device Technology Inc.

IDT 6116L AC CHARACTERISTICS-WRITE CYCLE (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

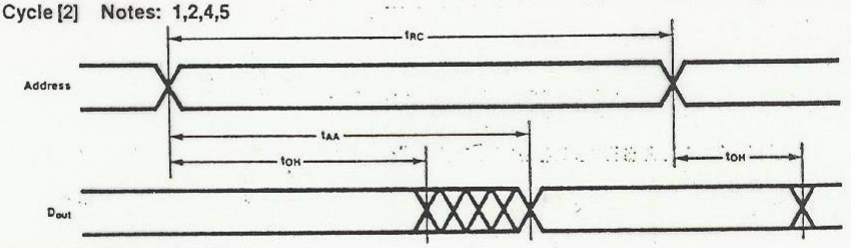
ITEM	SYMBOL	IDT6116L-90 MIN.	IDT6116L-90 MAX.	IDT6116L-120 MIN.	IDT6116L-120 MAX.	IDT6116L-150 MIN.	IDT6116L-150 MAX.	UNIT
Write Cycle Time	t_{WC}	90	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	55	—	70	—	90	—	ns
Address Valid to End of Write	t_{AW}	80	—	105	—	120	—	ns
Address Set-up Time	t_{AS}	15	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	55	—	70	—	90	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	40	0	50	ns
Write to Output in High Z	t_{WHZ}	0	50	0	50	0	60	ns
Data to Write Time Overlap	t_{DW}	30	—	35	—	40	—	ns
Data Hold from Write Time	t_{DH}	5	—	5	—	10	—	ns
Output Active from End of Write	t_{OW}	0	—	5	—	10	—	ns

TIMING WAVEFORMS

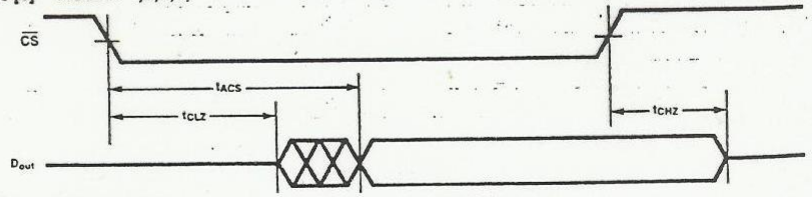
Read Cycle [1] Notes: 1,5



Read Cycle [2] Notes: 1,2,4,5



Read Cycle [3] Notes: 1,3,4,5,



NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

CAPACITANCE (1) (T_a = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	8	pF	$V_{I/O}$ = 0V

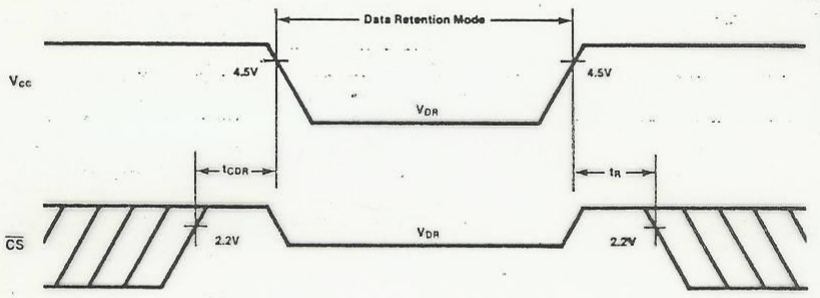
NOTE: 1. This parameter is sampled and not 100% tested.

IDT 6116L LOW VCC DATA RETENTION CHARACTERISTICS (T_a = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ = V_{CC} V_{IN} = 0V or V_{CC}	2.0	—	—	V
Data Retention Current	I_{CCDR}	V_{CC} = 2.0V, $\overline{CS}$ = V_{CC} V_{IN} = 0V or V_{CC}	—	—	20	µA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		*t_{RC}	—	—	ns

*t_{RC} = Read Cycle Time

IDT 6116L LOW VCC DATA RETENTION WAVEFORM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Voltage on any pin with respect to Gnd	V_{in}	−0.5 to +7.0	V
Operating Temperature	T_a	0 to +70	°C
Storage Tempertature	T_{stg}	−55 to +125	°C
Temperature under bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_t	1.0	W

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.
Supply Voltage	V_{cc}	4.5	5.0	5.5
	Gnd	0	0	0
Input Voltage	V_{IH}	2.2	3.5	6.0
	V_{IL}	−1.0*		+0.8
Output Load	C_L			100
	TTL			1

(T_a = 0 to +70°C) *Pulse Width: 50ns, DC: V_{IL} min =

IDT 6116S DC CHARACTERISTICS (V_{CC} = 5V ± 10%, Gnd = 0V, T_a = 0 to 70°C)

ITEM	SYMBOL	TEST CONDITIONS	IDT6116S-70 MIN.	IDT6116S-70 TYP.*	IDT6116S-70 MAX.	IDT6116S-90/120 MIN.	IDT6116S-90/120 TYP.*	IDT6116S-90/120 MAX.	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = Gnd to V_{cc}	—	—	10	—	—	10	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = Gnd to V_{cc}	—	—	10	—	—	10	µA
Operating Power Supply Current	I_{cc}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	50	100	—	40	80	mA
	I_{cc1}	V_{IH} = 3.5V, V_{IL} = .6V $I_{I/O}$ = 0mA	—	40	—	—	35	—	mA
Average Operating Current	I_{cc2}	Min. Cycle, duty = 100%	—	50	100	—	40	80	mA
Standby Power Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS} \geq V_{cc}$ − .2V, $V_{IN} \geq V_{cc}$ − .2V or $V_{IN} \leq$ .2V	—	20	2000	—	20	2000	µA
Output Voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

*V_{cc} = 5V, T_a = 25°C

AC TEST CONDITIONS

Input pulse levels: 0.8V to 2.4V
Input rise and fall times: 10ns
Input and output timing reference levels: 1.5V
Output load: 1TTL gate and C_L = 100 pF (including scope and jig)

IDT 6116S AC CHARACTERISTICS-READ CYCLE (V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

ITEM	SYMBOL	IDT6116S-70 MIN.	IDT6116S-70 MAX.	IDT6116S-90 MIN.	IDT6116S-90 MAX.	IDT6116S-120 MIN.	IDT6116S-120 MAX.
Read Cycle Time	t_{RC}	70	—	90	—	120	—
Address Access Time	t_{AA}	—	70	—	90	—	120
Chip Select Access Time	t_{ACS}	—	70	—	90	—	120
Chip Selection to Output in Low Z	t_{CLZ}	5	—	5	—	10	—
Output Enable to Output Valid	t_{OE}	—	50	—	65	—	80
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	10	—
Chip Selection to Output in High Z	t_{CHZ}	0	35	0	40	0	40
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	40
Output Hold from Address Change	t_{OH}	5	—	5	—	10	—