Lecture / Laboratory #6

•Review major points from Lecture 5

•Review laboratory work (demonstrations)

•**Operational Amplifiers (Op-Amps)**

- Differential Ampl.
- Summing Ampl.
- Integrators and Differentiators

•**Sample – and Hold (S & H) ckt.**

- QUAD Bilateral Switch
- JFET (Junction Field Effect Transistor)
- MOSFET (Metal-Oxide-Semiconductor FET)

•**Analog Computer**

Lab.: Construct analog computer and measure $\theta(t)$ for

$\omega = 10^4$ sec^{-1}

LM124/224/324/SA534-F,N
LM324-D

DC ELECTRICAL CHARACTERISTICS $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

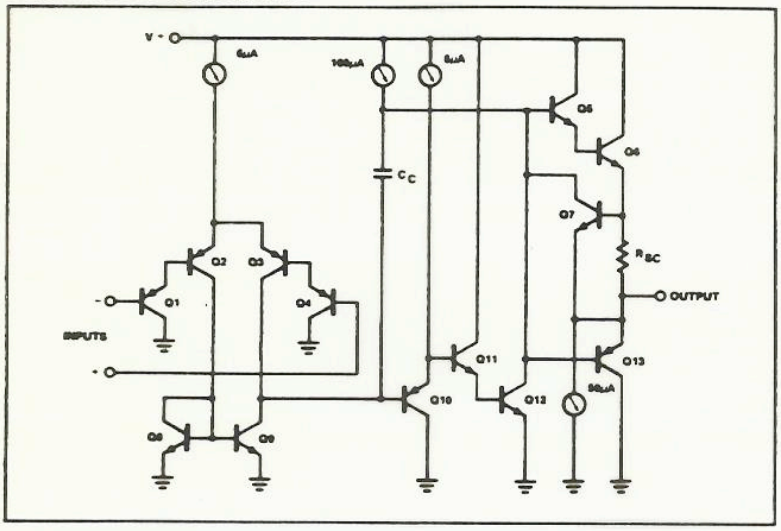
PARAMETER		TEST CONDITIONS	LM124/LM224			LM324/SA534			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	$R_S = 0\Omega$		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ $I_{IN}(+)$ or $I_{IN}(-)$, over temp.		45 40	150 300		45 40	250 500	nA nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$ $I_{IN}(+) - I_{IN}(-)$, over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift			10			10		pA/°C
V_{CM}	Common mode voltage range[3]	V+ = 30V V+ = 30V, over temp.	0 0		V+−1.5 V+−2	0 0		V+−1.5 V+−2	V V
C_{MRR}	Common mode rejection ratio		70	85		65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, V+ = +30V, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp.	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, V+ = 5V, over temp.		5	20		5	20	mV
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp. $R_L = \infty$, on all op amps, over temp.		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
A_{VOL}	Large signal voltage gain	V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$ V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	50 25	100		25 15	100		V/mV V/mV
	Amplifier-to-amplifier coupling[5]	f = 1kHz to 20kHz, input referred		−120			−120		dB
P_{SRR}		$R_S \leq 0\Omega$	65	100		65	100		dB
	Output current Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	5	8		5	8		mA
		$V_{IN}+ = 0Vdc$, $V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

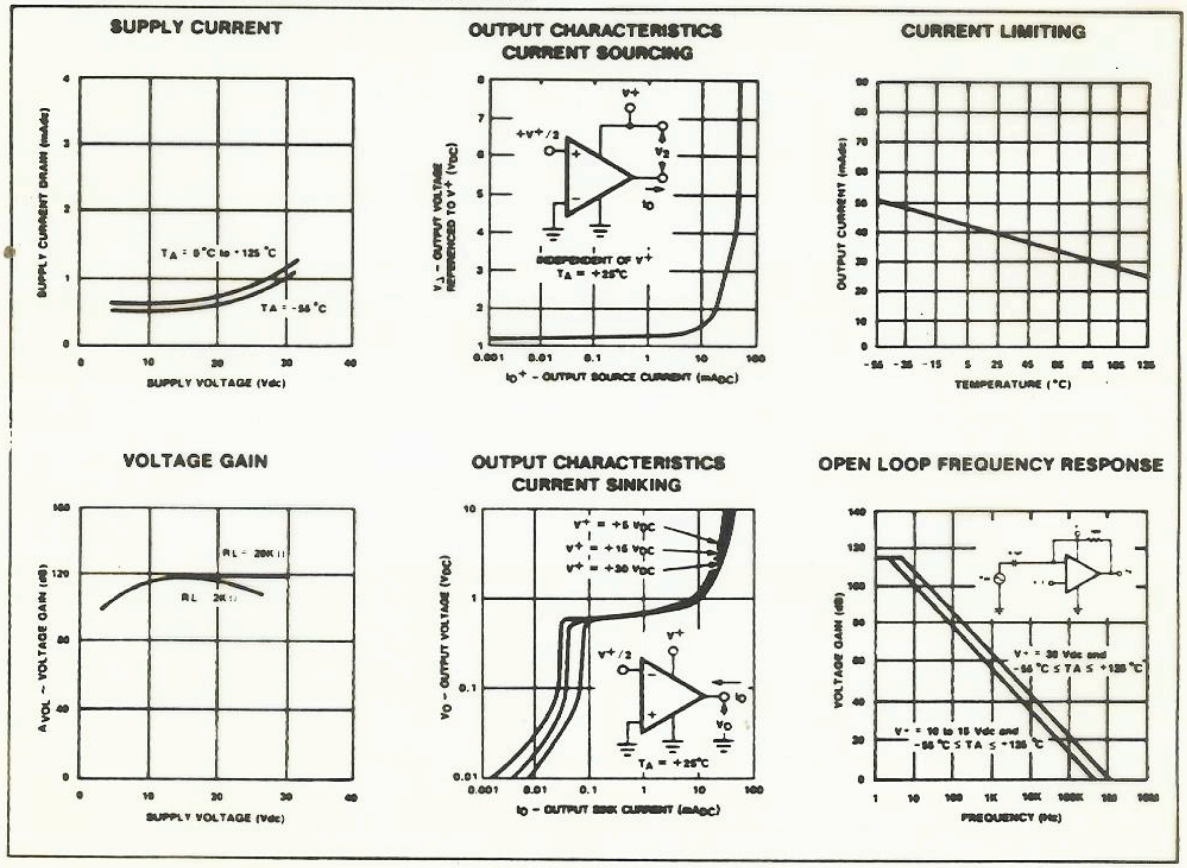
1. $V_O = 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ −1.5V)
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +32Vdc without damage.

LM124/224/324/SA534-F,N
LM324-D

EQUIVALENT SCHEMATIC



TYPICAL PERFORMANCE CHARACTERISTICS



GENERAL PURPOSE SINGLE SUPPLY OPERATIONAL AMPLIFIER

LM124/224/324/SA534

LM124/224/324/SA534-F,N
LM324-D

DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

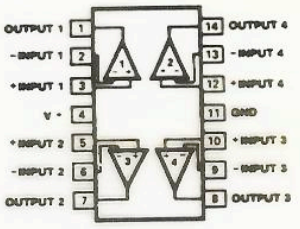
The input bias current is also temperature compensated.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  - **Single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)**
- **Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nAdc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nAdc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—1.5Vdc swing)**
- **LM124 Mil std 883A,B,C available**

PIN CONFIGURATION

D,F,N PACKAGE



ORDER PART NO.

LM124N	LM224N	LM324N
LM124F	LM224F	LM324F
SA534N	SA534F	LM324D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V+	Supply voltage	32 or ±16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation[1]		
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier[2]	Continuous	
	V+ < 15Vdc and T_A = 25°C		
	Input current (V_{IN} < -0.3V)[3]	50	mA
	Operating temperature range		
	LM324	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

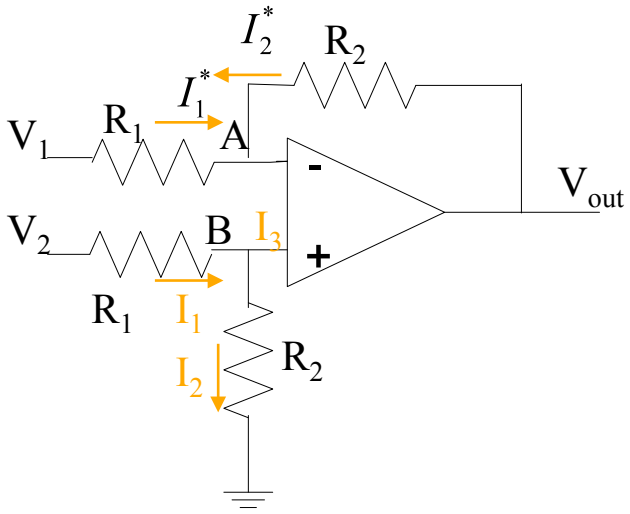
1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM 124/224 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

Differential Amplifier

$V_A = V_B$ ← 1st golden rule

$I_1 + I_2 + I_3 = 0$ at point B

$I_3 = 0$ ← 2nd golden rule



$$I_1 = (V_2 - V_B)/R_1 \qquad I_2 = V_B/R_2 \qquad |I_1| = |I_2| \longrightarrow \frac{V_2 - V_B}{R_1} = \frac{V_B}{R_2}$$

$$V_B\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{V_2}{R_1} \Longrightarrow V_B = V_A = V_2\frac{R_2}{R_1 + R_2}$$

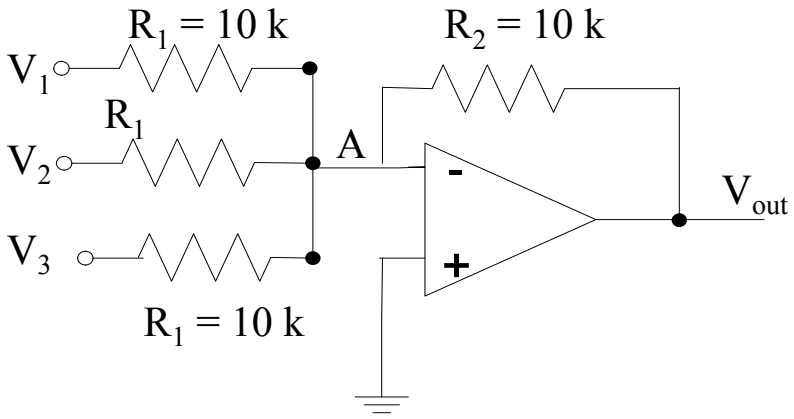
$$I_1^* = -I_2^* = \frac{V_1 - V_A}{R_1} = \frac{V_A - V_0}{R_2}$$

$$V_0 = \frac{R_2}{R_1}V_A + V_A - \frac{R_2}{R_1}V_1 \Rightarrow V_0 = \frac{R_2 + R_1}{R_1} \times \frac{R_2}{R_1 + R_2}V_2 - \frac{R_2}{R_1}V_1$$

$$\boxed{\frac{V_0}{V_2 - V_1} = \frac{R_2}{R_1}}$$

Summing Amplifier (Voltage Summation)

Point A is at virtual ground.



Hence:

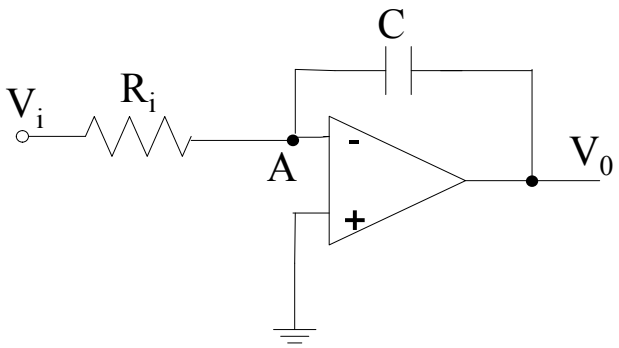
$$\frac{V_1}{R_1}+\frac{V_2}{R_1}+\frac{V_3}{R_1}=-\frac{V_0}{R_2} \Rightarrow V_0=-(V_1+V_2+V_3+\ldots)\frac{R_2}{R_1}$$

If $R_2 = R_1$ $\longrightarrow$ $\boxed{V_0=-(V_1+V_2+V_3+\ldots)}$

Note that inputs can be positive or negative. If resistors R_1 are not equal, the sum will be weighted sum.

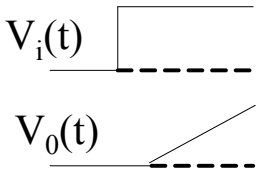
Integrators

Op-amp allows to make nearly perfect integrator, without the restriction that $V_0 << V_i$



$$I_i = \frac{V_i}{R_i} = -I_0 = -C\frac{dV_0}{dt} \Rightarrow \boxed{V_0 = -\frac{1}{R_i C}\int V_i dt + const.}$$

$$V_0(t) \sim \int V_i(t)dt$$



Some problems:

(a) Leakage current in op-amp

(b) Offset of $V_0(t)$

Solutions:

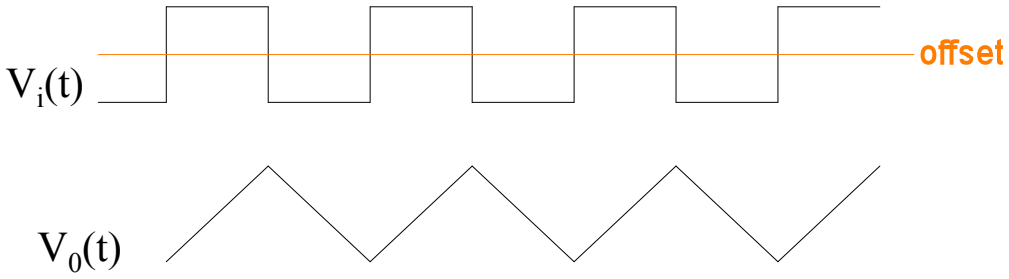
For (a) → choose very large C (but should be optimum, because impedance)

V = Q / C

$Q = \int Idt$ → small ΔI (leakage) doesn't really change Q, hence $V_0(t)$

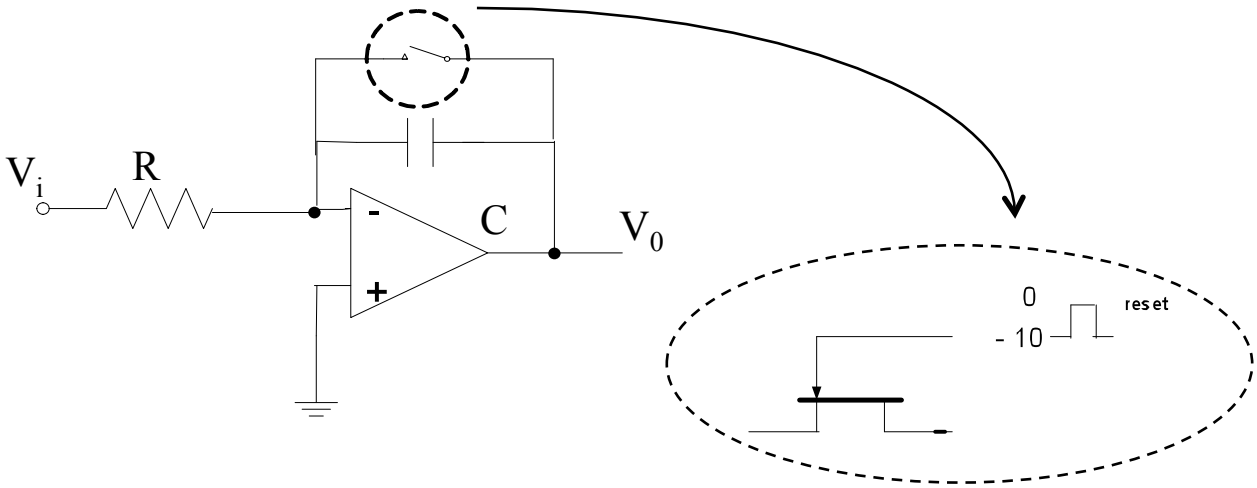
Integrators (cont.)

Solution for (b) → choose offset on square wave to compensate for $V_0(t)$ offset



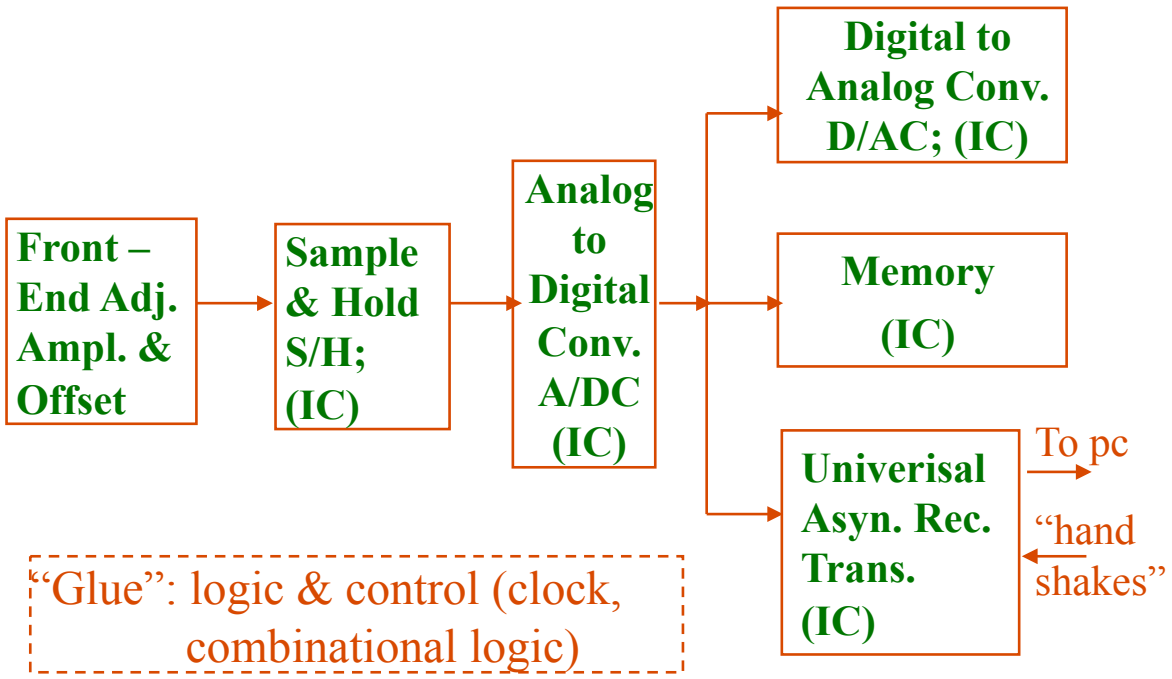
Note offset of $V_0(t)$ even with input grounded (virtual ground).

Integrator can be zeroed periodically by closing the switch across capacitor C (usually an FET n – channel JFET)



Digital Sampling Oscilloscope (DSO)

Block diagram:



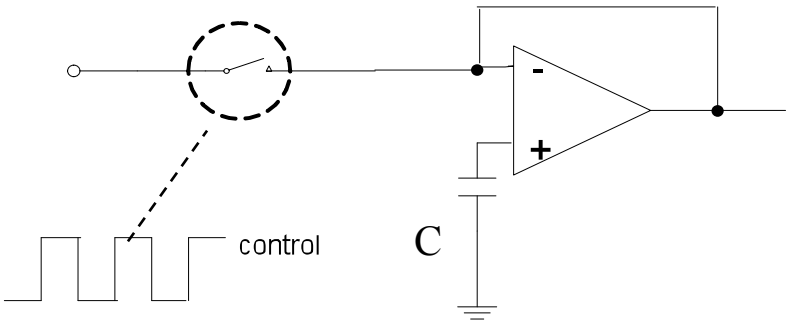
Modes of Operation ⟹

1. Acquisition Mode (Memory) →Not fast
2. Display Mode (Reading from memory) → Fast
3. Transfer Mode ← Slow

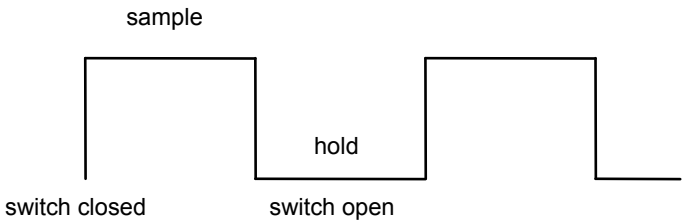
Sample – and – Hold Circuit

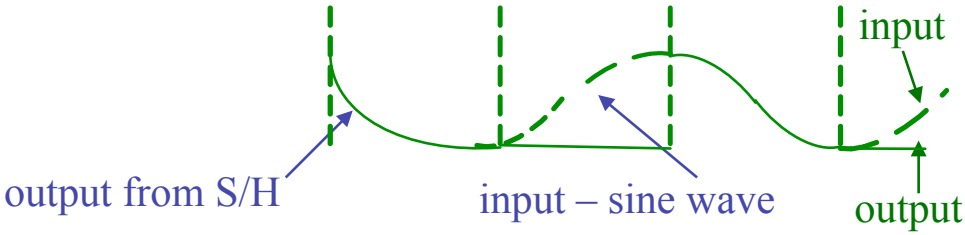
An analog switch which when closed passes the local voltage to the other side is the basis ofr a sample – and – hold ckt. The control signal drives the switch "on" and "off".

When switch is closed, the ckt "samples" what is on line, and when open, it "holds" the voltage there, so eq. A/D converter can perform an operation on it.

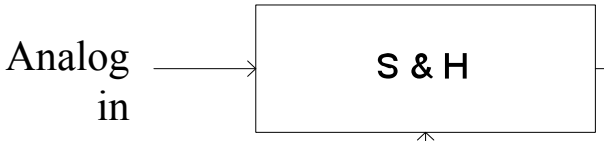


C should be such that it will provide good source impedance and sample time (As large as possible, but not too large for input impedance).





S & H Circuit (cont.)

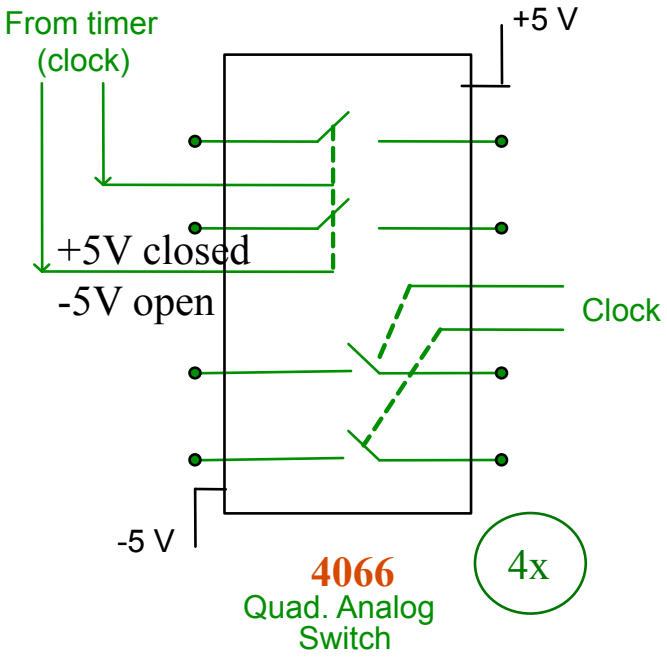


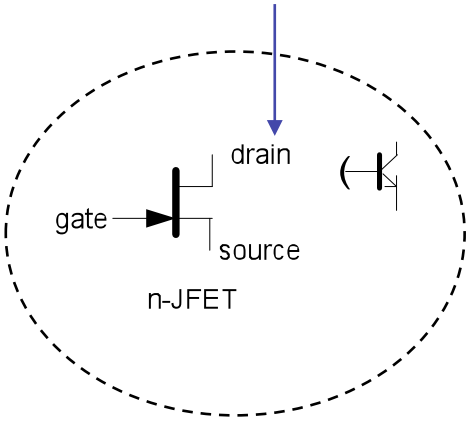
Digital logic control

⇓

Clock from time (: example 555 IC)

\+ switch : example ⇒ 4066 Quad Analog Switch (4JFET)

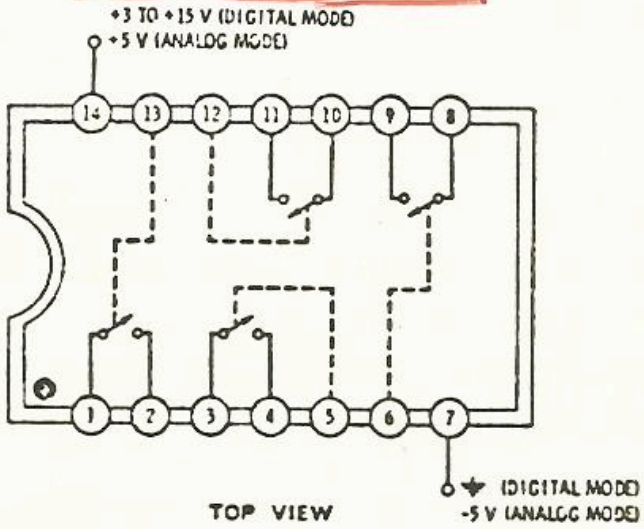




Junction Field Effect Transmission

4066

QUAD DIGITAL OR ANALOG BILATERAL SWITCH



TOP VIEW

All four switches may be used separately or in combination.

On any single switch, when the control voltage equals the pin-7 voltage, the switch remains OFF and behaves as a very high impedance. When the control voltage equals the pin-14 voltage, the switch turns ON and behaves as a nearly linear, bilateral, 90-ohm resistor.

Signals routed through the switch may be digital or analog, but they must never exceed the pin-14 voltage nor go below the pin-7 voltage.

Switches may be shorted together in any pattern, and there is no difference between the input and output terminals of any switch.

For instance, if all four switches are connected with one common terminal, the package may be used as a 1-of-4 data selector, a 1-of-4 data distributor, a 1-of-4 analog commutator, or a 1-of-4 analog multiplexer.

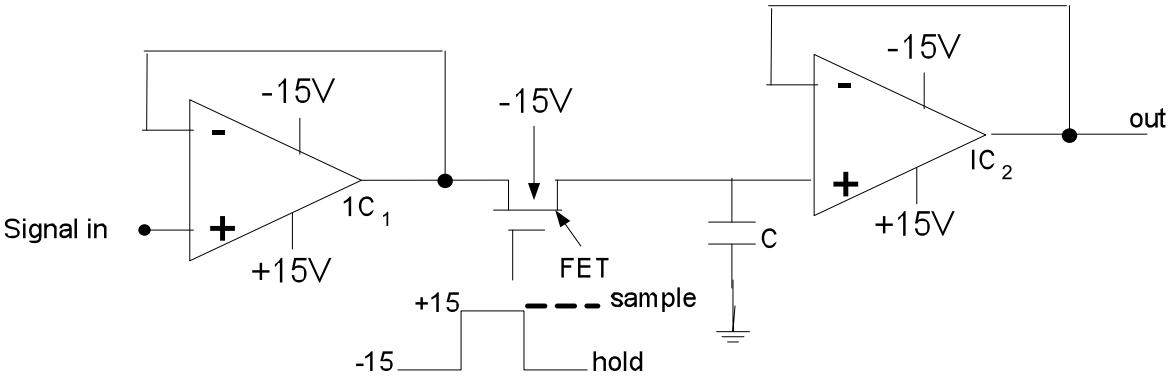
If more than one switch is connected to a common point, external logic usually must guarantee that only one switch is turned on at a time.

Maximum switching frequency is 10 megahertz at 10 volts and 5 megahertz at 5 volts. Package dissipation depends on the loading. Dissipation should be kept under 100 milliwatts total.

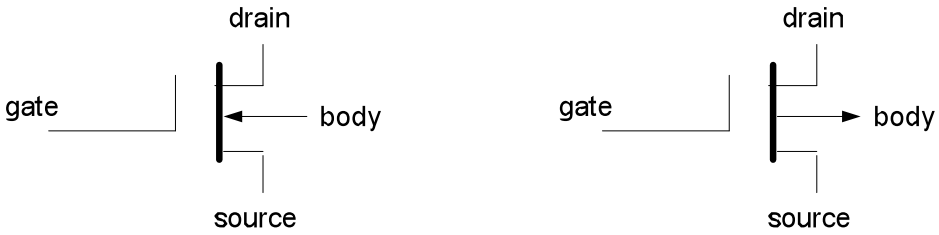
This is an improved version of the 4016, having a lower on resistance. However, the 4016 remains a better choice for ultralow-leakage applications such as sample-hold circuits.

See Chapter 7 for more information.

MOSFET



Sample – and – hold circuit with FET switch (MOSFET)



n - channel

p - channel

The insulated – gate FET or MOSFET ⇒ metal-oxide-semiconductor FET.

MOSFET (cont.)

JFET – gate forms a diode junction with the drain-source channel.

Leakage current (~nA), which increases with increasing drain voltages.

For forward – biased gate in respect to drain or source ⇒ regular diode construction.

MOSFET - gate is separated from the conducting channel by thin SiO_2 layer ⇒ hence, input resistance (on gate) $> 10^{14}\ \Omega$ (MOSFET is called insulated gate). Gate electric field effects channel conduction → MOSFET very sensitive to static electricity (easily damaged by touching it). Operates at any polarity on gate (without current on gate).