Lecture/Lab # 17 & 18

- Lab Review
- Lecture Review

- Memory (ROM)
- Elements of Digital Sampling Oscilloscope – Connections

  - Front – End (see lecture #8)

  - A/D Converter

  - Tri-State Bus ⇒ A/DC, D/AC, RAM (ROM), UART and Computer connections

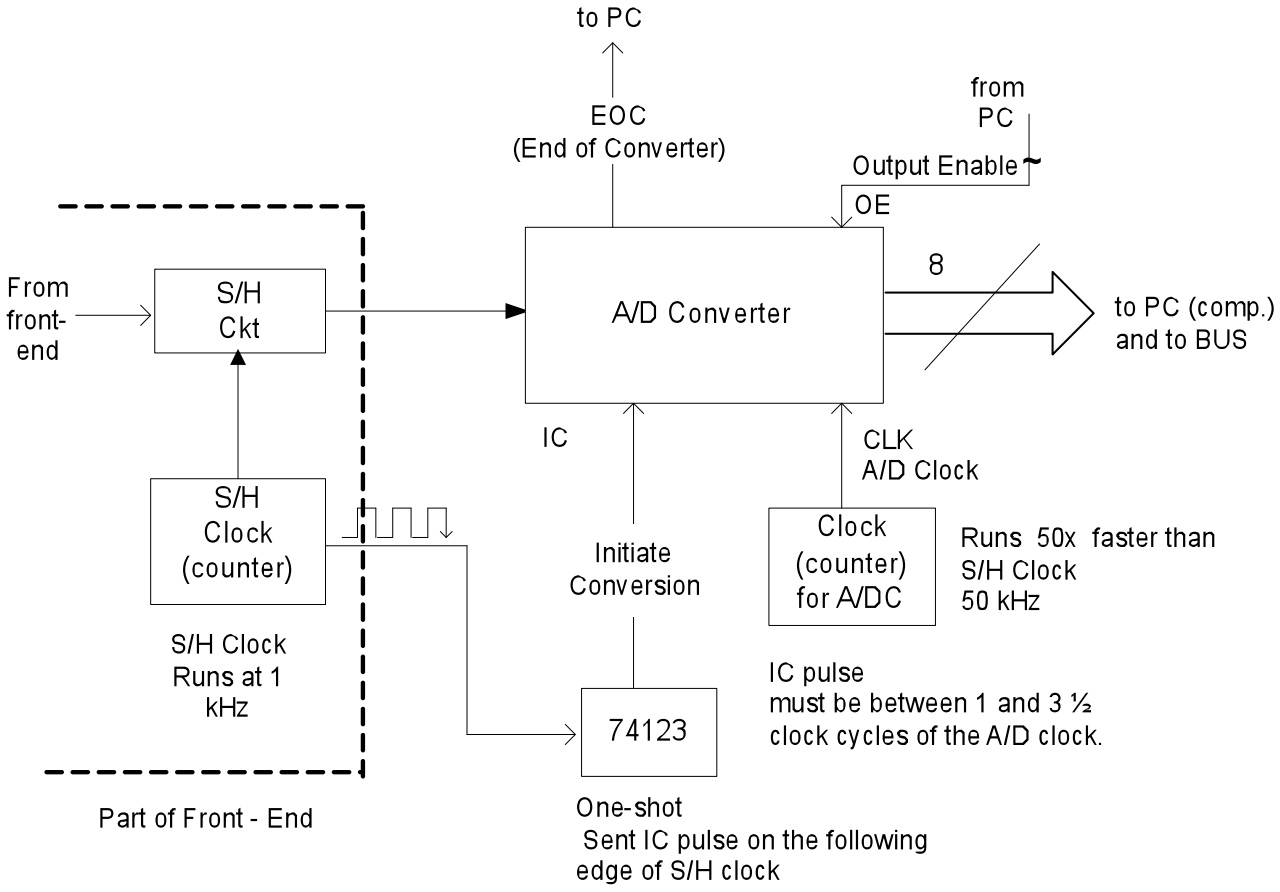
- **Discussion of Construction of Digital Sampling Oscilloscope (DSO)** (see also lecture #13)

Discussion of Elements of Digital Sampling Oscilloscope (DSO)

Front – End → see Lecture 8

Important to use appropriate sampling rate ⇒ clock (which may be one for all system) rate has to be properly divided to fit to S/H rate

A/C Converter



DSO (cont.)

A/D Conv. (cont.)

The analog signal from the output of front – end (S/H circuit) goes to A/D converter.

A/DC will convert analog signal into 8-bit digital word. The word will be sent from the A/DC through the controlling microprocessor to the data latch and into the RAM.

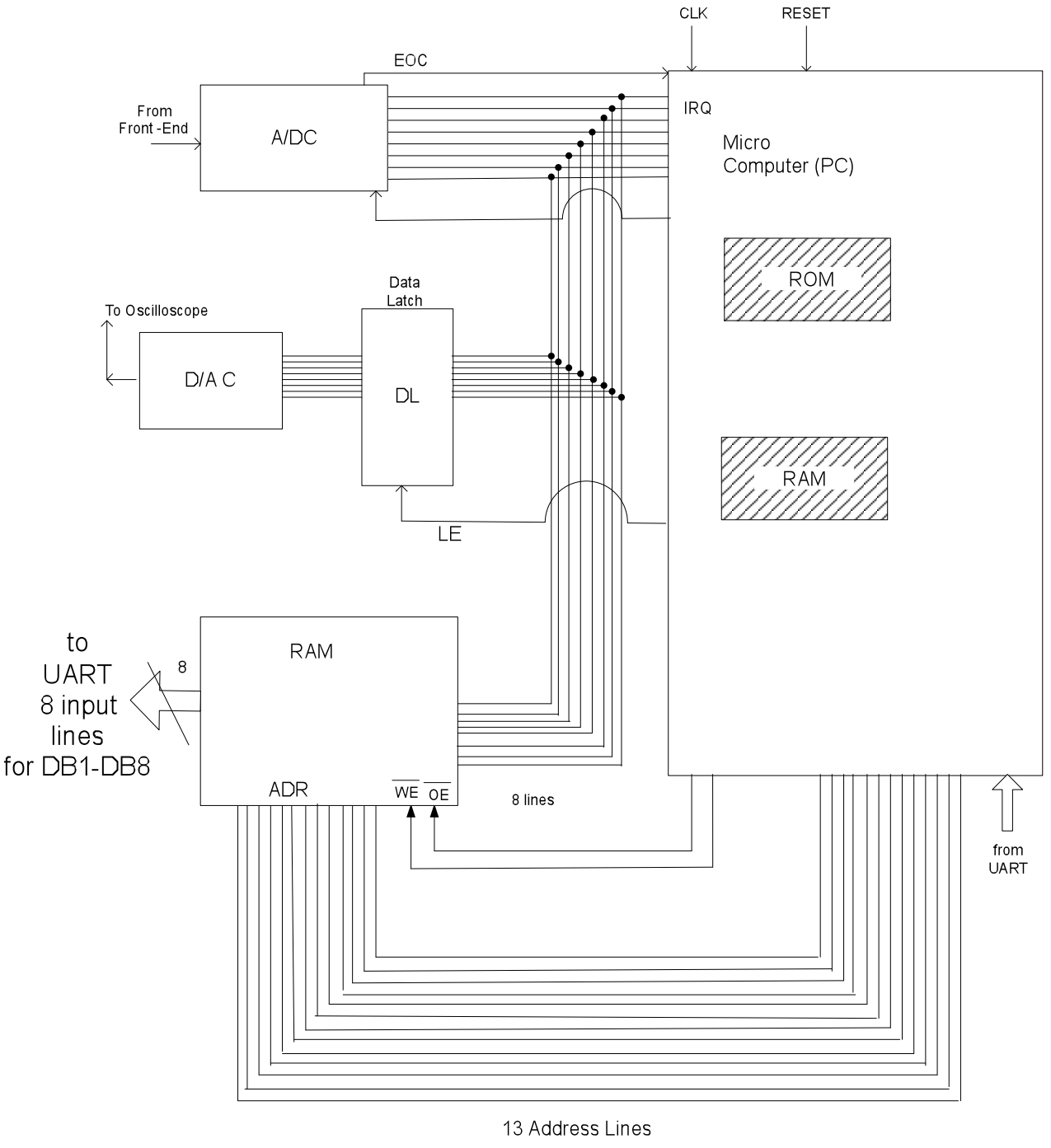
It requires 40 clock cycles to get converted signal in A/DC -800 (804 requires >70 clock cucles) by successive approximations.

Tri – state Bus

The A/DC, D/AC, Data Latch, RAM (ROM), and PC computer will be connected to the Tri-state bus (under control of the computer) that will master sequence of the acquisition and transmission of data throughout the process

DSO (cont.)

Tri – state Bus



Discussion of Construction of Digital Sampling Oscilloscope (DSO)

Remembering about manual coverage of:

- features (also location of elements on board)
- table of contents
- specifications (e.g. data sampling rates)
- principle of operation and function of major elements

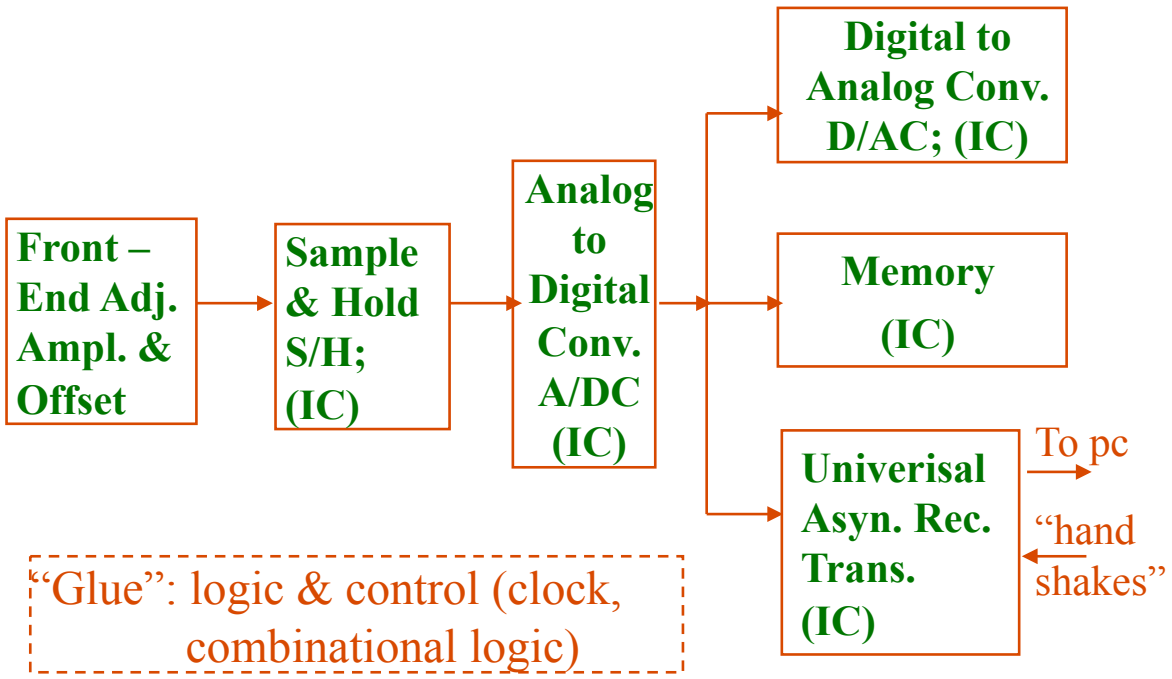
Different schemes possible (equivalent) (see examples)

Principle of design and construction

- calculation of clock rates for different parts of DSO
- compactness

Digital Sampling Oscilloscope (DSO)

Block diagram:



Modes of Operation ⟹

1. Acquisition Mode (Memory) →Not fast
2. Display Mode (Reading from memory) → Fast
3. Transfer Mode ← Slow

DSO construction (cont.)

Attention to:

- Possibility to view digitized signal directly (not stored)
  ⇒ digitized signal to D/AC and from D/AC to oscilloscope
- Playing back data from memory
- Calibration ⇒ known voltage on input → adjustment of gain and offset until output voltage = input voltage.

Analysis of one of the schemes

Input signal processing:

From unity gain op-amp signal goes to analog switch (4066), which switches the signal between two S/Hs → one is sampling, another is holding (avoid limitations for capacitor charging)

DSO construction (cont.)

Analysis of one of the schemes (cont.)

The outputs from S/Hs go to another et of analog switches (the same 4066), which combine two S/Hs signals ⇒ signal goes to another op-amp, which is also buffer between front-end and A/DC.

Bit rate generator MC 14411 provides clocking for 4066.

Conversion:

A/DC ⇒ ADC 0800. Clock for A/DC → from MC 14411. Minimize noise in ADC 0800 (wiring) and eliminate spikes (use capacitors for HF filtering: e.g. 4.7 μF capacitor).

Zero and full scale calibration for A/DC ⇒ "0" – by adding resistor (e.g. 680 Ω) to pin 5; 11111111 to 11111110 transition for 0.5 LSB voltage (~ 20 mV for 10 V input scale).

Full Scale – resistor to pin 15 (e.g. 1.5 kΩ);

00000001 → 00000000 transition for 1.5 LSB from full scale

DSO construction (cont.)

MC 14411 → 1.84 MHz crystal → 614.4 kHz clock → A/DC is clocked at 614.4 kHz and at 12.8 kHz or 9.6 kHz conversion clock (48 or 64 cycles, respectively for single conversion; 2 – 4 cycles for initiation conversion → between conversion).

Buffering by using inverted gates.

Conversion start by one – shot made of two FFs (can be done e.g. with timers or counters).

Conversion clock (12.8 or 9.6 kHz) is divided by 2 in another D – FF and it is used to switch 4066 for driving two S/Hs (Q and $\overline{Q}$ from D – FF). Conversion has to start after S/H switching (with appropriate delay in order to avoid interference with switching).

Signal to and from the RAM:

RAM with adjustable storage rate (instead of adjustable a/DC sampling rate) ⇒ low frequency signal can be stored in the limited memory without filling it too quickly.

DSO construction (cont.)

Variable storage rate ⇒ RAM clock and address counters dividing by 2^0, 2^1, 2^2, 2^3, etc. and using data selectors to choose the desired rate of operation of RAM.

End of Conversion (EOC) and Start Conversion (CVN) are two clocks from A/DC to divider/data selectors (‘151) and to RAM.

EOC clock’s rising edge is synchronized with the completion data conversion and EOC’s falling edge – with rising edge of the next start conversion pulse. EOC clock leads SC by 8 cycles (13μs) – guarantee stability of address in RAM during writing