PDP-8 Computer and Teletype ASR-33 Programming Info

Panel Switches

Name	Function
PANEL LOCK	Disables all switches except Switch Register.
MEM PROT	Prevents modification of memory locations 7600 - 7777. Also prevents JMS, DCA, ISZ instructions and input transfers.
DATA FIELD	Usage of this switch is enabled when Extended Memory is equipped.
INST FIELD	Usage of this switch is enabled when Extended Memory is equipped.
SWITCH REGISTERS	Input for LOAD ADDR and DEP. Also input for OSR instruction.
LOAD ADDR	Set current memory location to the address specified by the Switch Registers.
START	Initiates program execution from the current memory location. Clears Accumulator, Link, and Memory Buffer before execution.
CONT	Continues program execution from the current memory location. Does not clear Accumulator, Link, and Memory Buffer before execution.
STOP	Stops program execution.
SING STEP	When set, computer proceeds one instruction at a time with each press of CONT.
EXAM	Displats contents of current memory location in Memory Buffer. Then increments current address by 1.
DEP	Loads the Switch Registers value into the current memory location, which is displayed in Memory Buffer. Then increments current address by 1.

Instruction Set and Memory Architecture

PDP-8 uses 12-bit Octal (Eight) code for instructions and memory address.

4096 memory locations in total.

Absolute address range in octal: $0000 - 7777_8$

Memory is divided into pages of 200_8 memory locations each.

Page (Octal)	Memory Locations	Page (Octal)	Memory Locations	Page (Octal)	Memory Locations	Page (Octal)	Memory Locations
0	0-177	10	2000-2177	20	4000-4177	30	6000-6177
1	200-377	11	2200-2377	21	4200-4377	31	6200-6377
2	400-577	12	2400-2577	22	4400-4577	32	6400-6577
3	600-777	13	2600-2777	23	4600-4777	33	6600-6777
4	1000-1177	14	3000-3177	24	5000-5177	34	7000-7177
5	1200-1377	15	3200-3377	25	5200-5377	35	7200-7377
6	1400-1577	16	3400-3577	26	5400-5577	36	7400-7577
7	1600-1777	17	3600-3777	27	5600-5777	37	7600-7777

See Switch Registers on Front Panel of PDP-8 for bit alignment.

0	1	2	3	4	5	6	7	8	9	10	11
Opcode			I	Z	Address Offset						

I: 0 is Direct Addressing, 1 is Indirect Addressing (Pointer)

Z: 0 is Page 0, 1 is Current Page

- The 7-bit Address Offset can access the 200_8 memory locations within a page.
- Page 0 is accessible from any location by setting Z to 0; used for constants and pointers.

Indirect addressing: The 12-bit data content specified by the Address Offset is read as an absolute address for the instruction; treated as a pointer.

Table of Instructions

Machine Code	Mnemonic	Description
0xxx	AND	Logical AND with Accumulator, result in Accumulator.
1xxx	TAD	Two's Complement Addition with Accumulator, result stored in Accumulator.
2xxx	ISZ	Increment data content of memory location “xxx” and Skip next instruction if result is Zero.
3xxx	DCA	Deposit (Store) and Clear Accumulator, in memory location “xxx”.
4xxx	JMS	Jump to Subroutine. The return address is stored in memory location “xxx”. Control is set to the next instruction after “xxx”.
5xxx	JMP	Jump to memory location "xxx".
6xxx	I/O	General-purpose input-output operations.
7xxx	“Operate”	General-purpose operations.

“Operate” instructions are divided into 2 groups. Instructions within the same group can be combined into a single instruction.

“Operate” Opcode Group 1

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR/RTR	RAL/RTL	0/1	IAC

Bit	Mnemonic	Description
3	-	0 specifies that the instruction is in Group 1.
4	CLA	Clear the Accumulator.
5	CLL	Clear the Link.
6	CMA	Complement the Accumulator.
7	CML	Complement the Link.
8	RAR/RTR	Rotate the Accumulator and Link right; LSB of Accumulator rotates to Link.
9	RAL/RTL	Rotate the Accumulator and Link left; Link rotates to LSB of Accumulator.
10	-	0: Rotate 1 place (RAR, RAL) / 1: Rotate 2 places (RTR, RTL)
11	IAC	Increment the Accumulator.
3~11	NOP	No Operation. Bits 3-11 set to 0. (Code: 7000)

Order of Execution of Combined Group 1 Instructions

1) CLA, CLL
2) CMA, CML
3) IAC
4) RAR, RAL, RTR, RTL

"Operate" Opcode Group 2

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA/SPA	SZA/SNA	SNL/SZL	0/1	OSR	HLT	0

Bit	Mnemonic	Description
3	-	1 specifies that the instruction is in Group 2.
4	CLA	Clear the Accumulator.
5	SMA/SPA	Skip on minus/positive Accumulator. Next instruction is skipped if Accumulator is negative/positive.
6	SZA/SNA	Skip on zero/non-zero Accumulator. Next instruction is skipped if Accumulator is zero/non-zero.
7	SNL/SZL	Skip on non-zero/zero Link. Next instruction is skipped if Link is non-zero/zero.
8	-	0: SMA, SZA, SNL / 1: SPA, SNA, SZL; Determines the effects of Bits 5-7.
9	OSR	Logical OR of Switch Register and Accumulator, result in Accumulator.
10	HLT	Halt the computer.
11	-	0 specifies that the instruction is in Group 2.
5~7	SKP	Unconditional Skip. Bits 5-7 set to 0 with Bit 8 set to 1. (Code: 7410)

Combination of Group 2 Instructions

SMA, SZA, SNL conditions are ORed. (OR conditions)
(Accumulator < 0 || Accumulator == 0 || Link == 1)

SPA, SNA, SZL conditions are ANDed. (AND conditions)
(Accumulator >= 0 && Accumulator > 0 && Link == 0)

Order of Execution of Combined Group 2 Instructions

1) OR conditions / AND conditions
2) CLA
3) OSR
4) HLT

Auto-Index Memory Locations

Memory Locations: 0010 – 0017
Whenever used as a pointer by Indirect Addressing, will automatically pre-increment contents.
Can be used as an automatically pre-incrementing index for arrays and other similar structures.

Teletype Input/Output Transfer Instructions

0	1	2	3	4	5	6	7	8	9	10	11
Opcode			Device Selection Code						Operation Bits		

Opcode: 110, 6_8
Device Selection Code: 03_8 for input to computer, 04_8 for output to teletype.
Like "Operate" instructions, Operation Bits can be combined.

Input from Teletype Keyboard / Paper Tape Reader

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	0	0	0	0	1	1	KRS	KCC	KSF

Sequence	Mnemonic	Octal	Effect
1	KSF	6031	Skip the next instruction when the keyboard buffer register is loaded with an ASCII symbol (keyboard flag is set).
2	KCC	6032	Clear the Accumulator, clear the keyboard flag.
3	KRS	6034	Transfer the contents of the keyboard buffer to the Accumulator.
2, 3	KRB	6036	Transfer the contents of the keyboard buffer into the Accumulator, and clear the keyboard flag.

Output to Teletype Printer / Paper Tape Punch

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	0	0	0	1	0	0	TPC	TCF	TSF

Sequence	Mnemonic	Octal	Effect
1	TSF	6041	Skip the next instruction if the printer flag is set.
2	TCF	6042	Clear the printer flag.
3	TPC	6044	Load the printer buffer register with the contents of the Accumulator, print the character, and set the printer flag.
2, 3	TLS	6046	Clear the printer flag, transfer the contents of the Accumulator into the printer buffer register, print the character, and set the printer flag when done.

Note: Teletype does not print anything if Accumulator is cleared. (No Operation)

References

Introduction to Programming: PDP-8 Family Computers, Digital Equipment Corporation, 1968.